INFLUENCE OF DESIGN AND COATINGS ON THE MECHANICAL RELIABILITY OF SEMICONDUCTOR WAFERS

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ABSTRACT

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We investigate some of the mechanical design factors of wafers and the effect on strength. Thin, solid, pre-stressed films are proposed as a means to improve the bulk mechanical properties of a wafer.

Three-point bending was used to evaluate the laser scribe density and chemical processing effect on wafer strength. Drop and strike tests were employed to investigate the edge bevel profile effect on the mechanical properties of the wafer. To characterize the effect of thin films on strength, one-micron ceramic films were deposited on wafers using PECVD. Coated samples were prepared by cleaving and were tested using four-point bending. Film adhesion was characterized by notched four-point bending. RBS and FTIR were used to obtain film chemistry, and nanoindentation was used to investigate thin film mechanical properties. A stress measurement gauge characterized residual film stress. Mechanical properties of the wafers correlated to the residual stress in the film.

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CHAPTER 1: INTRODUCTION

Jack Kilby invented the integrated circuit (IC) in 1959.[1] In 2000, just 41 years after his invention, the US semiconductor industry had over $204 billion in net sales, and employed nearly 284,000 people.[2] For 2001, it is estimated that these same companies manufactured 60 billion transistors for every person on earth.

Today it is difficult to find any product that is not, in some way, connected to the industry. Nearly every manufactured item involves an IC, either in its creation or function. ICs are used in simple devices like watches and remote controls; they are used in complex devices such as computers, satellites, and space shuttles. And, at the very heart of the IC manufacturing process is the wafer fab.

The objective of this thesis is to focus on the mechanical properties of silicon to decrease the level of intrinsic wafer breakage in a wafer fab. This will be accomplished by 1) establishing some of the design and process contributions to intrinsic wafer breakage levels, 2) evaluating the effect of pre-fab processing techniques to breakage, 3) determining the influence of wafer edge design on breakage, and 4) identifying whether wafer coatings are a viable solution to improving the mechanical properties of silicon wafers.

The wafer fab is a complex manufacturing operation, contained within a low-particulate environment called a cleanroom. ICs are fabricated on round, highly pure, silicon disks called wafers. Multiple wafers make up a single manufacturing lot. Depending on the technology of the ICs produced, and the size of each wafer, the fab

may have capability to produce tens to tens-of-thousands of ICs per wafer. Further, fab output may be a few hundred to tens-of-thousands of wafers per month. The revenue generated from each wafer may be a few hundred to hundreds-of-thousands of dollars; again, this depends on the complexity of the IC. Naturally, a lower technology fab usually has a higher wafer run rate, but lower revenue generated per wafer, and vice versa. Using these numbers for rough calculations, the revenue generated per day by a single wafer fab may easily be in the range of a few million dollars, or close to a billion dollars a year.

Some factors affecting cost are included in Table 1.1.[3]

Table 1.1: Cost Elements for Producing a Finished Good Wafer.

Item	***Normalized Cost****
Starting wafer	20
Direct materials	12
Photomasks	
Chemicals	
Labor	12
Overhead	8
Overhead materials	8
DI water	
Gases	
Pilot wafers	
Other	
Depreciation	40
Facility	
Equipment	
Total	100

* Estimated values. Actual numbers will vary, depending on size and age of facility, utilization, product, etc.

Other ways to increase profitability are to minimize a lot's cycle time, or the time it takes to move a lot through the entire process, and maximize process yield, defined as the number of sellable wafers at the end of the line divided by the number of wafers started (minus any test wafers).

Both of the above profit-determining components are complex, usually involving many factors that must be balanced in order to obtain optimum performance. For instance, process yield has multiple contributors: a wafer's final electrical test yield, intrinsic wafer breakage levels throughout the process, process stability, and human error are a few examples.

The components of process yield that will be investigated in this work are factors affecting the mechanical strength of silicon wafers. Since the wafer itself is the foundation upon which all ICs are constructed, it is imperative that the wafer be designed to survive the process.

When first considering materials to use for coatings, one must understand the attention that is given to semiconductor reliability. Rarely will a new material be used without extensive testing. To minimize the amount of work that might be spent on reliability testing, and to maximize the time spent on the material mechanics, it is beneficial to use materials that have an extensive history. Silicon nitride, carbide, and oxide are materials and films already used in current semiconductor processing technology. Therefore, the reliability impact of these materials on semiconductor device operation is already established.

Second, it is true that both silicon and many ceramics are brittle; however, one should carefully consider the difference in mechanical properties between them. Experimentally, silicon is more brittle than most ceramics. Thus, it may be possible to capitalize upon the *relative strength* of the ceramic in strengthening the silicon.

Finally, and most importantly, one needs to bear in mind the processing environment that a typical wafer might experience. As will be discussed in the following chapters, wafers are commonly processed using wet processes. For this, the wafer is dipped in a bath that contains an etchant. Hydrofluoric acid (HF) is one chemical that is used to etch materials on wafers; in particular, it is used for oxides and nitrides. While it is unlikely that the coating would be etched completely in early baths, subsequent processing would be sure to remove the entire ceramic layer. Thus, any coating that may be used for mechanical strengthening purposes should be able to survive the entire wafer fab process. While oxides and nitrides may be useful in early stages of wafer processing, their usefulness is sure to deteriorate with subsequent wet etching. However, HF is not a good etchant for silicon carbide. Rather, this ceramic material is usually etched with an O_2/hydrocarbon RIE (reactive ion etch). The likelihood of this material surviving the process with the full benefit to the coating on the wafer is much greater with carbide than for the oxide or nitride.

To investigate the effect of design and coatings on silicon wafer mechanical strength, a number of topics will be discussed. Chapter Two of this work presents and discusses an overview of semiconductor device physics. A summary of present semiconductor manufacturing technology is provided in Chapter Three. In Chapter Four, material mechanics and strength testing techniques are presented. Post-failure analysis of wafers and a method to determine the origin of wafer fractures are presented in Chapter Five. Chapter Six presents the effect of barcode dot density and chemical etching on wafer mechanical strength; both isotropic and anisotropic chemical etches are

investigated. Next, in Chapter Seven, the design of silicon wafer edges and the effect on mechanical strength is discussed. General measures to improve wafer strength as a result of design changes are presented. In Chapter Eight, the use of ceramics as structural thin films for silicon wafers is proposed. Finally, in Chapters Nine and Ten, respectively, results will be summarized, and future work will identified.

Three-point bend tests determined the influence of wafer barcode design on mechanical properties. Wafer drop and strike tests were used to determine the effect of edge bevel design on mechanical strength at the wafer edge. Four-point bend tests were utilized to characterize the effect of thin film (~1μm) residual stress upon bulk silicon mechanical properties. Film stress was found using commercially available equipment, and scanning electron microscopy (SEM) and optical microscopy (OM) techniques were used to provide images of samples.

CHAPTER 2: SEMICONDUCTOR DEVICE PHYSICS

2.1 Overview

A semiconductor is a material that has limited conductive properties, but not enough to be considered a conductor. Conductivity is defined in Equation 2.1 below:

$$\sigma = en\mu_e \tag{2.1}$$

Where e is the charge of the electron, n is the number of charge carriers, and μ_e is the drift mobility of the electron through the material. Table 2.1 provides the electrical conductivity ranges for various types of electrical materials.

Table 2.1: Electrical Conductivity of Materials

Type of Material	Electrical Conductivity (S/cm)
Insulator	10^{-20}-10^{-8}
Semiconductor	10^{-8}-10^{2}
Conductor	10^{2}-10^{6}
Superconductor	0

For intrinsic semiconductors, conductivity follows Equation 2.2:

$$\sigma = e(n_e\mu_e + n_h\mu_h) \tag{2.2}$$

In this case, e, n_i (where i = e or h for electron or hole) and μ_e are the same as before; μ_h is the drift mobility of a hole through the semiconductor. Semiconductors pass charge through the movement of either electrons or holes, so both need to be accounted for in the calculation. For intrinsic semiconductors the number of electrons must equal the number of holes to conserve charge; therefore n_e must equal n_h. The intrinsic conductivity of pure crystalline silicon at room temperature is given to be $2.9\text{x}10^{-6}$ S/cm, putting it in the semiconductor range.

Electronic grade silicon is the most prevalent semiconductor material in use today. Since crystalline silicon is comprised of atoms with four valence electrons (Figure 2.1) each covalently bonded to an electron from a neighboring atom, we can make use of it for semiconducting purposes. It is not the covalent bond that causes semiconducting properties in silicon, but rather the ability for "free" electrons to move in the presence of an electric field.

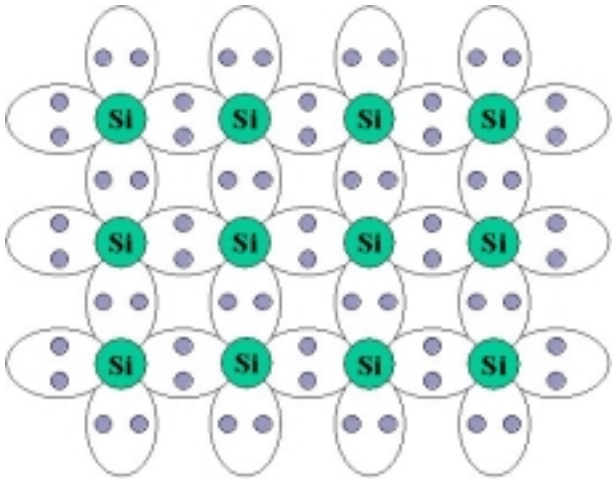


Figure 2.1: Silicon semiconductor

Through the introduction of a small number of impurities (usually with an element having a valency of three or five) in an otherwise pure silicon crystal, the conductivity of the semiconductor can be changed. Generally, the addition of these impurities raises the conductivity of the material. This new material is known as an extrinsic semiconductor. Extrinsic semiconductors exist because the added impurity replaces a silicon atom from the crystal lattice.

There are two types of extrinsic semiconductors: p-type and n-type. In n-type semiconductors, the dominant charge carrier is the electron, and the added impurity contains five valence electrons instead of four, as in silicon. The impurity has an extra

electron. This extra electron can roam through the material, but overall charge neutrality is maintained since a local (bound) positive charge exists at the impurity site due to the loss of the electron. Figure 2.2 represents n-type silicon semiconductors.

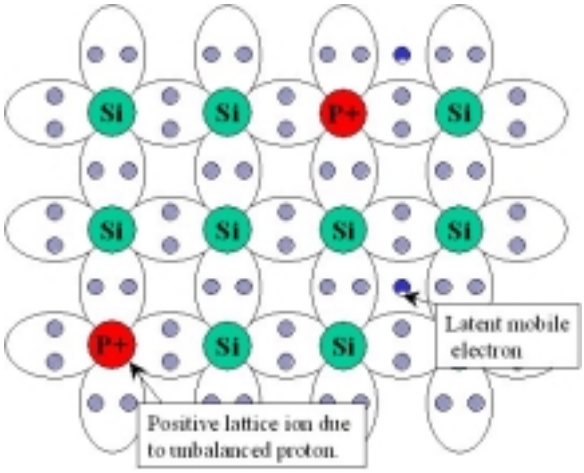


Figure 2.2: N-type silicon semiconductor

Examples of n-type impurities are phosphorus (P), arsenic (As), and antimony (Sb).

In p-type semiconductors, the dominant mobile charge carrier is the hole, and the impurity contains only three valence electrons. Since there are only three bonding electrons, this creates a roaming positive charge in the lattice, but a local negative charge at the impurity site. Figure 2.3 represents p-type silicon semiconductors.

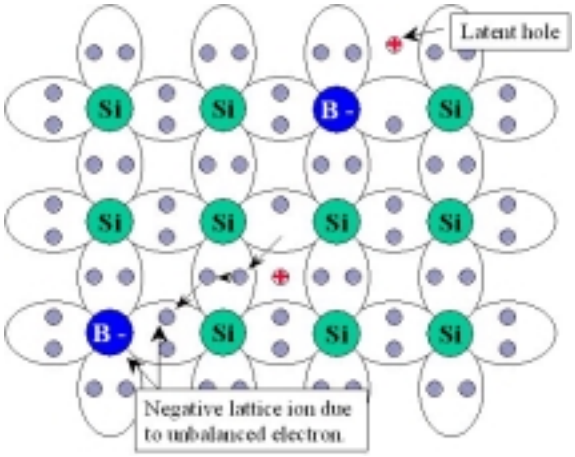


Figure 2.3: P-type silicon semiconductor

The most commonly used p-type impurity is boron (B).

For a doped silicon crystal, it is important to know how Equation 2.2 changes. For n-type silicon, the dominant charge carrier is the electron. Thus, conducting electrons in the solid will greatly outnumber the number of holes (i.e., $n_e >> n_h$). For this reason, the conductivity of n-type silicon is closely approximated as shown in Equation 2.3.

$$\sigma \approx e n_e \mu_e \tag{2.3}$$

For p-type silicon, the opposite is true (i.e., $n_h >> n_e$). Thus, Equation 2.2 can now be approximated as shown in Equation 2.4.

$$\sigma \approx e n_h \mu_h \tag{2.4}$$

Equations 2.3 and 2.4 hold true only if the number of electron donors (N_d) or electron acceptors (N_a), respectively, is much, much greater than the number of intrinsic charge carriers. Since we typically talk about impurity levels in silicon on the order of 4×10^{13} atoms/cm^3 (1 ppb) or higher, Equations 2.3 and 2.4 are valid.

2.2 Semiconductor Devices

Applying an electric potential across the semiconductor will allow current to flow. Current flows when the mobile charge carrier (electrons for n-type silicon, and holes for p-type silicon) moves from one end of the material to the other, or in the corresponding direction of the applied field (opposite direction for electrons, same direction for holes). It is this principle that is used to create semiconductor devices.

2.2.1 Diodes

If one were to place p-type silicon directly next to n-type silicon, this would create a P-N junction. This junction is known as a diode. At the interface of the two materials, known as the metallurgical junction, electrons from the n-type region recombine with holes from the p-type region and form a depletion, or space charge, region. In the space charge region, there are fixed localized charges; however, the net charge is still conserved since one electron must combine with exactly one hole. This space charge region is depicted in the bottom image of Figure 2.4 below.

When an external bias is applied in the same direction as the internal charge of a diode, that is the same charge polarity in the space charge region, this is called reverse bias.

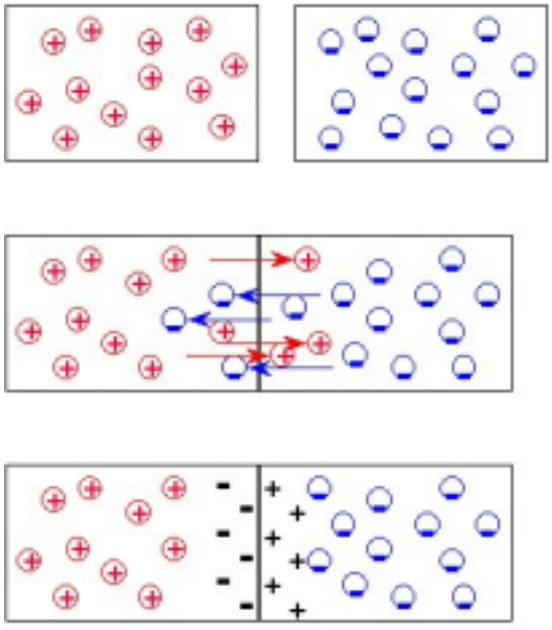


Figure 2.4: The P-N Junction

Reverse biasing a diode allows for negligible current flow, as the majority carriers in each region are pulled away from the P-N junction (Figure 2.5).

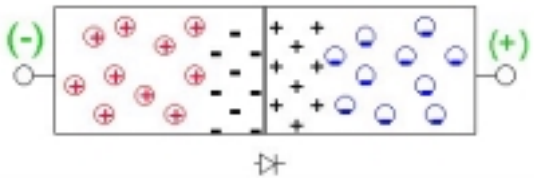


Figure 2.5: Reverse biased diode

Forward bias is the opposite of reverse bias, and charge carriers move closer to the junction. At a certain point, the forward threshold voltage, current begins to flow. Hole drift occurs in the p-type region; electron drift happens in the n-type region; and recombination occurs near the junction. Charge carriers are injected at the terminals of each end of the device. Figure 2.6 shows the forward biased diode.

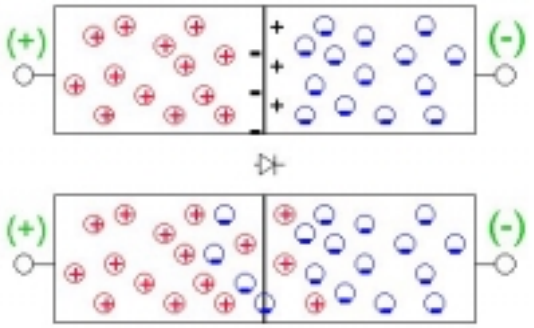


Figure 2.6: Forward biased diode

Placing two diodes back-to-back creates a device called a transistor. This NPN device, or PNP, can be used to regulate current flow (usually in "ON/OFF" positions, as in the digital world), and this is the benefit of the IC.

2.2.2 Transistors

There are three fundamental types of transistors, but only two will be discussed here. The junction field effect transistor, or JFET, will be omitted because it is not very commonly used in the industry.

The first transistor that will be discussed is the bipolar junction transistor (BJT); it consists of three alternating layers, either NPN or PNP. The regions are called emitter, base, and collector, respectively.

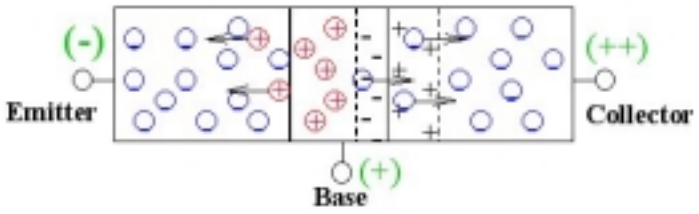


Figure 2.7: Bipolar Junction Transistor (BJT)

To turn a transistor on, one junction, the emitter-base, is forward biased; the other junction, the base-collector, is reversed biased (Figure 2.7). Charge carriers are injected from the emitter into the base in the reverse-biased diode, pass through the very thin base into the space charge region of the reverse-biased base-collector junction, and carried into the collector. Transistor action is the name of this effect. In the NPN transistor of Figure 2.7, holes move into the emitter and recombine, and the input current to the base region replenishes them. For a PNP BJT, the electron/hole flow and positive/negative voltages in Figure 2.7 would be reversed.

The other type of semiconductor transistor is the metal-oxide-semiconductor field effect transistor, or MOS-FET. The name MOS comes from the original device construction; a *metal* "gate" was placed on top of a thin *oxide*, which was on top of the *semiconductor*. Current technology may use other materials for gates and oxides, but the naming convention still remains today.

This transistor also consists of three functional regions: the source, gate, and drain. In the MOSFET, the source and drain are both either n- or p-type doped silicon.

The channel region is the opposite type of silicon as the source and drain. For an n-type source and drain we have an NMOS transistor; for p-type we have a PMOS transistor.

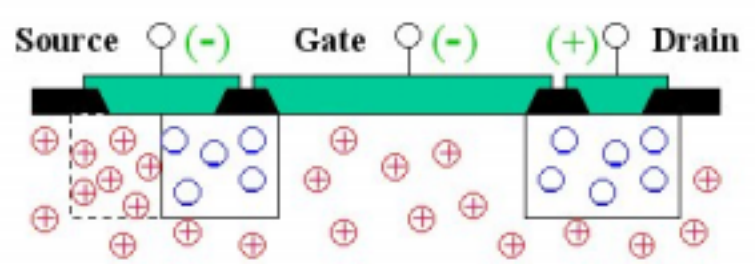


Figure 2.8: NMOS Field Effect Transistor

Figure 2.8 shows the representative structure of an NMOS transistor. The very thin oxide layer – between tens and hundreds of angstroms thick, depending on technology – spans the channel between source and drain. The oxide is thin to allow electrostatic interaction between the gate and semiconductor, and ultimately control of the channel. If no bias or negative bias is applied to the gate in an NMOS transistor, no current flows from source to drain.

As the voltage on the gate is increased, it reaches a threshold voltage, V_t. At V_t the holes under the gate are repelled from the semiconductor-oxide interface to form a depletion region. Increasing the voltage past V_t attracts electrons into the depletion region, thereby forming a thin electron layer, or inversion layer; current can now flow between source and drain. Figure 2.9 shows the open MOSFET transistor.

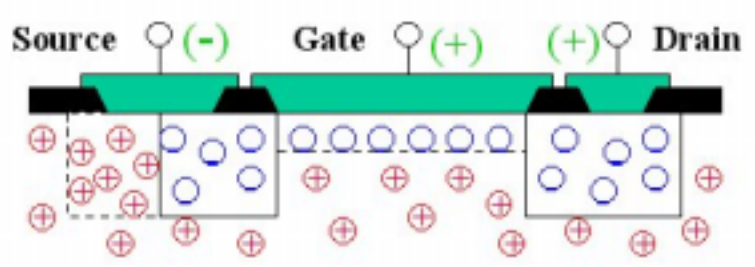


Figure 2.9: Open NMOS Field Effect Transistor

As the gate bias is increased, the channel becomes deeper, and more electrons are pulled into the inversion layer. The PMOS version of the NMOSFET is exactly opposite in terms of electrons/holes and voltages.

As a side note, it is also possible to make a transistor where a channel exists with no bias on the gate. Such a transistor is called a depletion mode MOS transistor, and it stays on until turned off. To turn it off, a negative bias must be applied to the gate (for an NPN). However, this transistor construction is not very commonly used.

In the discussion of diodes and transistors, the basic building blocks of the IC have been covered. And, it is with the careful arrangement of these structures on the wafer that a microchip is created. Through careful fab processing, the device physics of a structure are modified to create the desired electrical effect.

CHAPTER 3: SEMICONDUCTOR PROCESSING OVERVIEW[4]

Wafer fab processing requires a series of different steps, none too trivial in nature. Depending upon complexity, a single chip may be large (>400 mm^2) or small (<1 mm^2); it may have one layer of metal or multiple layers; the wafer may take as little as a week or as long as a few months to complete the manufacturing process. But, no matter the complexity, size, or cycle time to fabricate the finished device, the type of processing used to create these devices is fundamentally similar.

3.1 Wafer Processing

Wafers are grown in a single crystal silicon ingot from a melt by either a pulling (Czochralski or Teal-Little) method or a float zone (FZ) process. The Czochralski (CZ) method is the most commonly used method in the production of semiconductor grade silicon, and almost no FZ-grown crystals are used in the production of silicon ICs. FZ-processing is more common in the production of other semiconductor wafer materials and when the highest purity wafers are required.

When pulling a crystal, a single-crystal silicon seed is dipped into the silicon melt and slowly rotated. If one controls the temperature of the melt and the amount of heat removed from the seed, freezing onto the seed (growth) is possible. Typical seed diameters may be in the range of a few millimeters, but the final ingot diameter may exceed 300mm. The change in and control of the diameter required for crystal growth are accomplished by varying the melt temperature, seed crystal spin rate, and seed pull

rate. Increasing the melt temperature will decrease the crystal diameter; increasing the pull rate decreases the diameter; and increasing the rotation rate increases the diameter.

Since the crystal growth process requires a very different set of equipment from IC manufacturing very few, if any, semiconductor companies produce their own silicon wafers anymore. Wafer production is confined to a few major companies; MEMC, Wacker, Shin-Etsu, and Mitsubishi are a few of them. Figure 3.1 shows the various stages of the crystal pulling process.

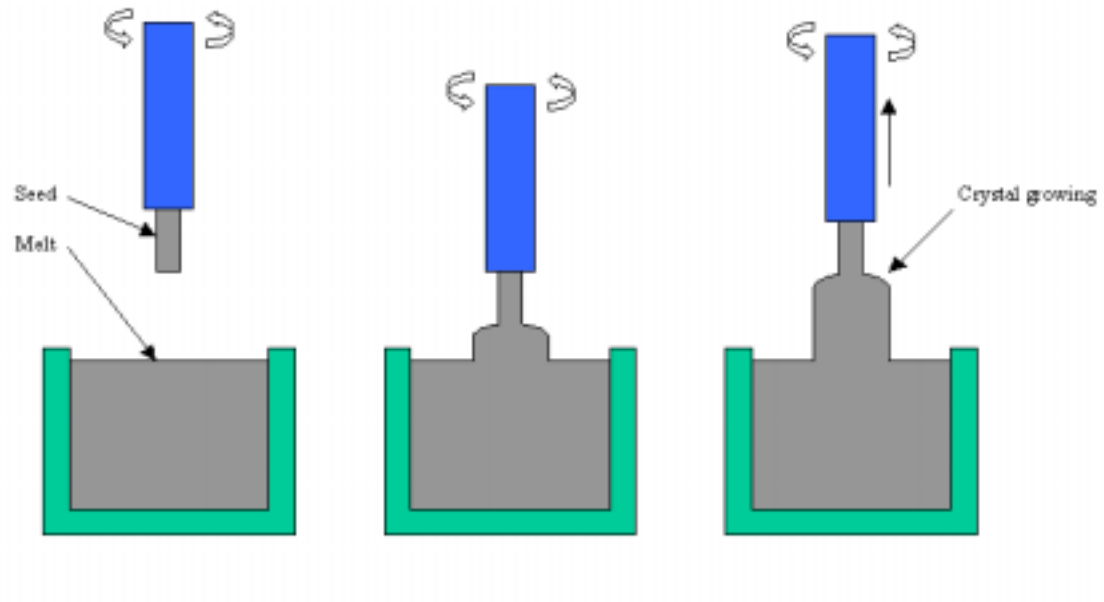


Figure 3.1: Various stages of crystal pulling from the melt

After the crystal has been pulled, the crystal ingot is taken through various mechanical shaping operations to produce the final polished wafer slice. First, the ends of the as-grown crystal are cut off and the ingot is ground to remove undulations so that all the wafers will have the same diameter. Next, an orienting flat or notch is ground into the ingot before it is sawed into slices. Third, the edges of the wafer are rounded or beveled to reduce edge chipping. SEMI Standards, documents used by the

semiconductor industry, provide guidelines for, and among other things, the acceptable edge bevel profile range by wafer thickness. (The edge bevel can be a very important characteristic affecting wafer mechanical integrity; this will be discussed in greater detail later in this discourse). Finally, the slices are lapped with progressively smaller grits to remove fracture damage, polished on one or both sides, inspected, and shipped to the wafer fab. Figure 3.2 shows some of the mechanical shaping operations that occur in the crystal production area.

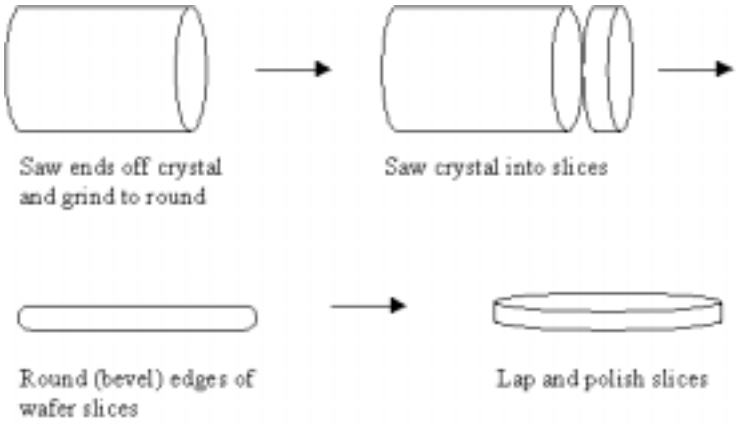


Figure 3.2: Mechanical shaping operations after the ingot is pulled

3.2 Semiconductor Processing

Fab processing can be broken into several major processing areas: surface cleaning, epitaxy, oxidation, impurity diffusion or implantation, photolithography, etching, deposition (CVD and PVD), multiprobe, and backgrinding. The order of these steps is not fixed; in fact, depending on the complexity or structure of the device being fabricated, a wafer may circulate through each step multiple times (see Figure 3.3).

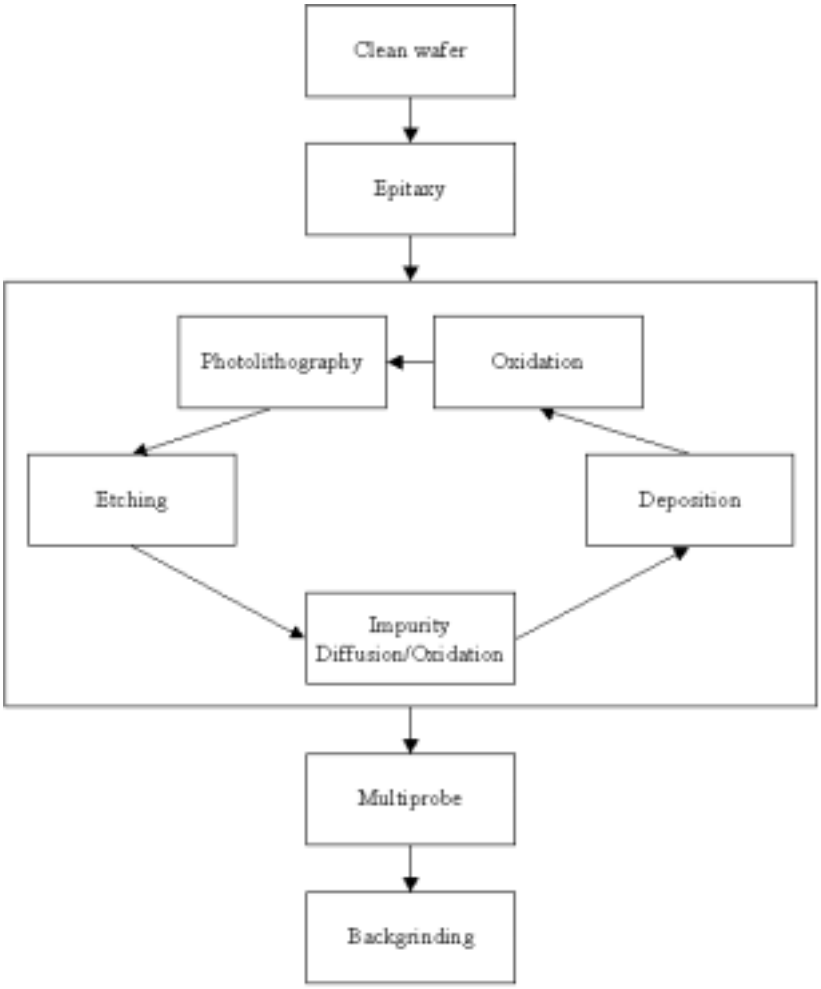


Figure 3.3: Summary of the Semiconductor Process Flow

For the sake of brevity, processing technology will only be covered in very general detail. Sze[5] and Van Zant[6] have presented in depth reviews.

3.2.1 Surface Cleaning

Almost always, the first step in the wafer manufacturing process involves cleaning the surface of the wafer. Wafers are cleaned to remove particulates, organic films, and adsorbed metal ions from the surface of the wafer; all can significantly reduce the electrical yield of the finished wafer. Simple cleaning involves the immersion of the wafer in a liquid or spray bath (acids, solvents, or ultra pure water); ultrasonic agitation

or brush scrubbing may also be used to increase the cleaning efficiency. A deionized (DI) water rinse is typically the final step in the cleaning process.

3.2.2 Epitaxy

Epitaxy (also, epitaxial growth or epi) is the growth of a thin layer of single-crystal material on a single-crystal substrate, usually silicon on silicon. The thin epi layer is usually doped so that it will be a different resistivity (usually higher to reduce transistor series resistance) than the bulk substrate. Epi growth is characterized to contain fewer total impurities than the underlying substrate, and depending on the device may be a few tenths of a micron to tens-of-microns thick.

Vapor phase growth is the most common silicon epi method, and employs high temperature (1000-1200^{o}C) reduction of a silicon-bearing compound at the surface of the wafer. Common reactions are the hydrogen reduction of $SiCl_4$, $SiHCl_3$ or SiH_2Cl_2 (dichlorosilane or DCS). Lower temperature growth may use the reduction of SiH_4. Layer doping employs the co-deposition of an appropriate impurity (e.g., P or B) through thermal reduction.

3.2.3 Oxidation

Thermal oxidation of silicon is usually performed between the temperature range of 800-1250^{o}C and in an oxygen or steam atmosphere using an inert carrier gas. In the oxidation reaction, silicon is immediately consumed from the surface of the wafer, and then at the silicon-oxide interface. Due to Fickian diffusion, the reaction rate changes over time given constant temperature and oxygen concentration. Also, for every micron

of oxide grown, 0.45 microns of silicon is consumed. Due to LeChatelier's Principle, increasing the partial pressure of oxygen increases the rate of the following reaction:

$$Si + O_2 \rightarrow SiO_2$$

This is often a viable way to reduce the oxidation time at lower temperatures.

3.2.4 Impurity Diffusion/Ion Implantation

Impurity diffusion and ion implantation are very similar in the end, but the means are fairly different. In diffusion, a source dopant is provided, and the oxidation process now becomes a diffusion process. The mass transfer mechanics of transferring an impurity directly from a gas ambient and into the wafer are inefficient. Thus, the process is generally designed to let the dopant react with silicon oxide on the surface of the wafer; the newly formed silicate glass becomes the impurity source for diffusion into the wafer.

The diffusion process is typically broken into two steps. In the first, a very thin, high-concentration dopant deposition, or "dep," is diffused at the wafer surface. The surface concentration of the dopant is set by the solubility limit of the dopant at the dep temperature. In the second step, the "drive," a different temperature is used to give the desired diffusion profile, or surface concentration and diffusion depth. In the diffusion furnace wafers are held by their edges in a long quartz or polysilicon tube, separated by a few millimeters in a quartz, polysilicon, or silicon carbide boat. Temperature control in the furnace is usually $\pm 1^{o}$C, and diffusion times vary from minutes to many hours.

Ion implantation is an alternative solution to the diffusion process. In implantation, the dopant atom is accelerated to a high velocity so that after the atom strikes the surface of the wafer, the atom continues into the wafer. The implanter uses

electric fields to accelerate the atom, thus ions must be used instead of atoms. Acceleration voltages range from a few thousand to a few million volts, and correspond to relative implant depths. Ion implantation may also be used in addition to diffusion to obtain depths greater than traditional implant alone. Regardless of the need for additional diffusion, a thermal heat treatment is required post-implant to anneal the crystal damage caused by the implant process and to activate the dopant by making it substitutional. For very high dosage implants, the damage may be so severe as to cause an amorphous layer at the wafer surface; they may be appropriately heated to epitaxially regrow the layer into a high-quality single crystal.

Implantation is typically much faster than diffusion. However, because of the highly specialized equipment required to implant a wafer, the incremental process cost is greater for an implant than it would be for the analogous diffusion process. The decision to implant or to diffuse is almost always a cost decision.

3.2.5 Photolithography

Photolithography is the name for the process in which a pattern of masking material called photoresist, or resist, is applied to the surface of a wafer. The purpose of the pattern is to provide protection to desired portions of the wafer and to allow material to be removed from the remaining area through etching. Figure 3.4 shows the steps in patterning an oxide wafer.

Resist, a photosensitive liquid, is applied to the wafer by dropping a metered amount onto the rotating wafer. The speed is then increased to a few thousand RPM's so that the resist is spun into a very thin, uniform layer (about a micron thick) by centrifugal

force. Exposing it to a high-intensity ultraviolet light source through a photomask develops the pattern in the resist; the light pattern is determined by the pattern on the mask.

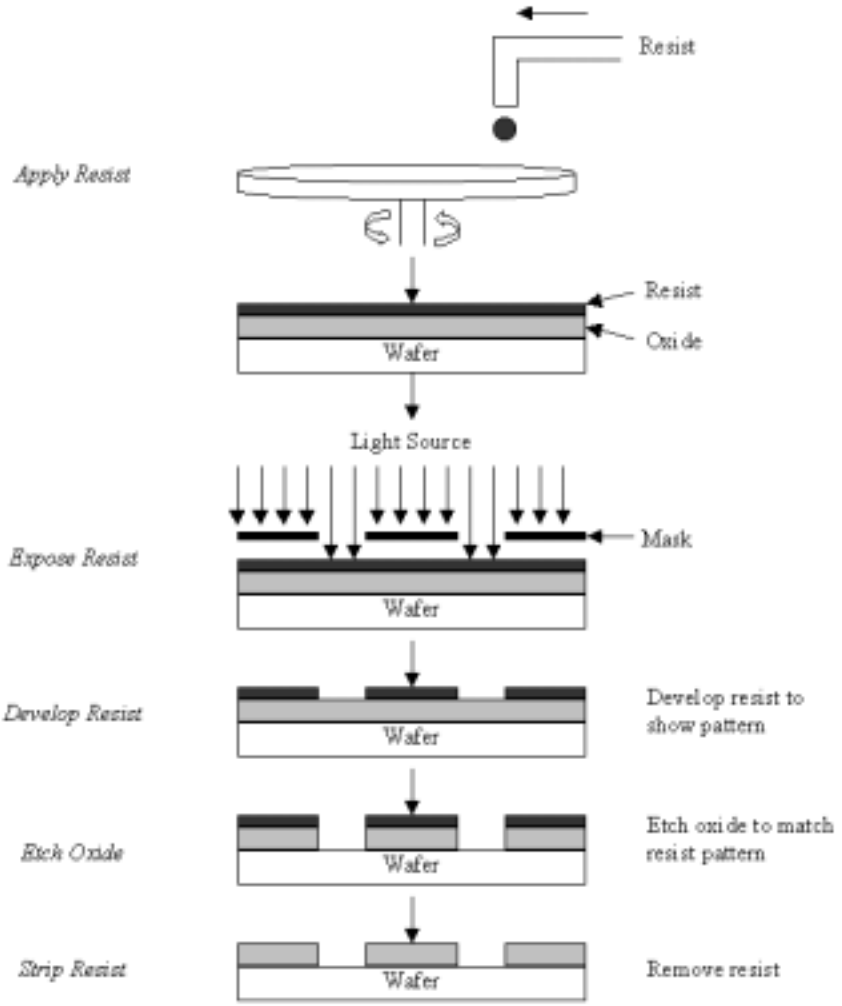


Figure 3.4: Photolithography steps in patterning an oxide

There are two main categories for photolithography in existence. In the first method, contact printing, the photomask comes in either close proximity (~1μm) to the wafer or in direct contact with the wafer prior to exposure. In contact printing, the photomask contains a 1:1 ratio in feature size on the mask to feature printed on the wafer. This method, however, is very dated, and only employed by a few older technology wafer

production facilities. In the second and more common method, the pattern is projected through a series of lenses and printed on the wafer. In this method, the mask to printed feature ratio may be 1:1, 5:1, or 10:1. If the mask feature is larger than the printed feature, the lenses will reduce the image to the appropriate size when printing. In the develop process, the unwanted resist is removed and leaves a pattern of the bare oxide, or other material, under the resist.

3.2.6 Etching

After exposing the pattern in the resist, the underlying material is removed by etching. The most common type of etching occurs through either an aqueous-based or a plasma-enhanced process. In either case, the etch must be stopped at the bottom of the layer being etched. While etch rate and time are characterized for each type of etch, these are not sufficient means to control the process. In addition to these controls, the etch chemicals are chosen to provide good selectivity between the etched and underlying material(s). Good selectivity ensures that all of the desired layer can be removed without removing a consequential amount of the underlying layer.

Plasma etching is preferred for smaller geometry features since it is typically considerably more anisotropic than wet etching. In this context, anisotropy refers to the nearly straight down etching characteristic through the pattern window. Wet etching is much more isotropic, meaning that the etch will occur in all directions equally. Figure 3.5 shows the sidewall profile difference between the two etch types. The dark top layer on the wafer is the photoresist, while the lighter layer is the layer to be etched.

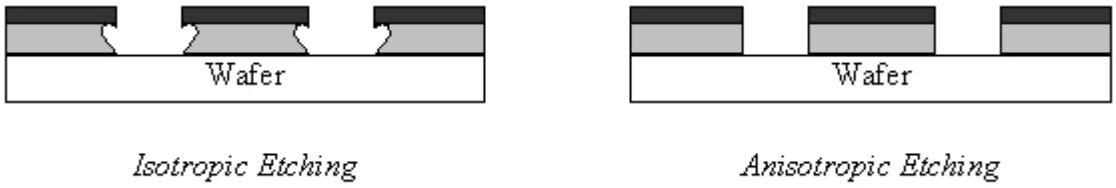


Figure 3.5: Sidewall profiles of isotropic etching versus anisotropic etching

As a side note, wet etching can also be classified as anisotropic, though in a slightly different sense of the term. Here, anisotropy refers to the tendency for some etch chemicals to preferentially etch along the silicon crystal lattice. Also known as orientation-dependent etching (ODE), the wet chemicals etch a crystal faster in planes where the packing density is less. For instance, [100] planes are much less dense than [111] planes in crystal silicon. An ODE etch will etch along the [100] planes much quicker than it will the [111] planes. Figure 3.6 shows the difference in ODE, or anisotropic, and isotropic etches.

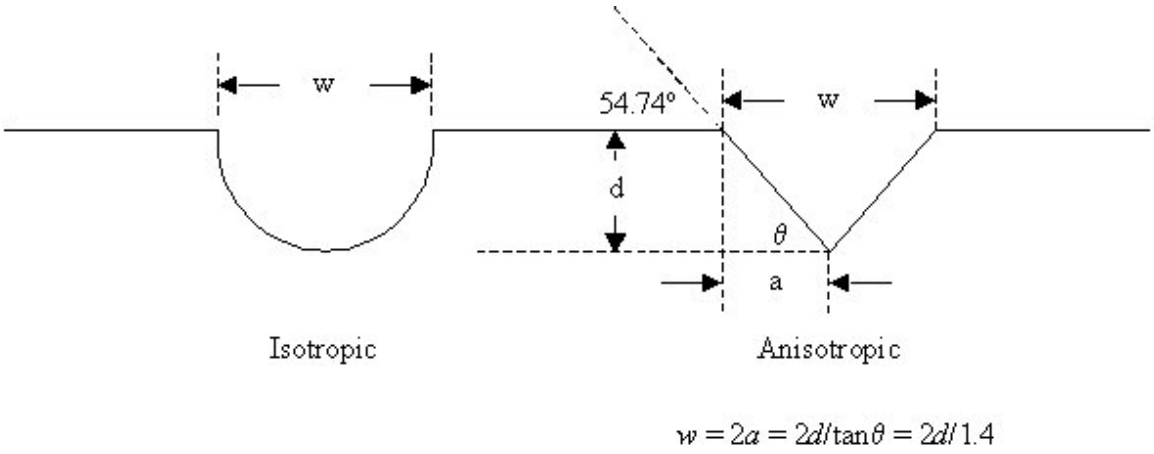


Figure 3.6: Wet chemical isotropic and anisotropic etching of silicon

Typical wet etch chemicals are HF-HNO_3 for silicon (isotropic), HF for SiO_2 and Si_3N_4, hot H_3PO_4 for silicon nitride, and cold H_3PO_4 for aluminum. Some reported ODE etch chemicals for silicon involve use caustic mixtures that may be composed of KOH and DI water mixtures, hydrazine and DI water or alcohol, and ethylenediamine and DI

water or alcohol. Plasma gases are usually freon based and contain chlorine or fluorine (e.g., CF_4).

3.2.7 Deposition (CVD and PVD)

Layer deposition in the semiconductor process often takes one of two forms: physical vapor deposition (PVD) and chemical vapor deposition (CVD). Each offers its own benefits, and each is equally employed in the process.

CVD is used to deposit layers like polycrystalline silicon and some metals in addition to ceramics like silicon and metal oxides, nitrides, and carbides. CVD temperatures may range between 300-900^{o}C, and the following reactions may be used:

$$SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$$

$$SiH_4 \xrightarrow[\Delta]{} Si + 2H_2$$

Oxides deposited in this way do not bond to the silicon surface as well as thermal oxides, and may have lower densities. Therefore, this deposition technique is not an alternative process, but an adjunct process to be used in cases when thermal oxidation temperatures would be deleterious to the materials already on the wafer (e.g., when depositing an oxide on top of a metal), or when an oxide is needed but there is no silicon to be oxidized.

Plasma-enhanced CVD (PECVD) processing can also be used. The main benefit of plasma-assisted depositions is that reactions that normally require much higher temperatures in order to progress can now be accomplished in lower temperature ranges; the plasma supplies a portion of the energy required in the reaction process. Silicon nitride is one example of a film than may be deposited using PECVD. Nitride PECVD

temperatures can be deposited at 300^{o}C, while straight CVD may require temperatures over 800^{o}C.

Physical vapor deposition (PVD) is the traditional means for depositing metal films on silicon wafers. PVD includes evaporation and sputtering. Evaporation is easy and inexpensive. Sputtering offers much better metal step coverage, and may be required to get acceptable deposition rates for refractory metals. Gold, platinum, titanium, tungsten, copper, molybdenum, palladium, chromium, and aluminum may all be employed; depending upon application, alloys may be used, too. Aluminum and its alloys are the most common metals in use, but copper is gaining ground because of its lower resistivity.

3.2.8 Multiprobe

Upon completion of fab processing, the chips on the wafer are individually tested and sorted. Multiprobe is the test operation to accomplish this task, and it uses a series of pointed probes that make electrical contact the bond pads (used for bonding electrical wires in the assembly operation to connect the die to the leadframe). In probe, a series of electrical tests are performed on the die to determine if it functions properly. An ink dot may be placed on the failing die to aide in subsequent sort operations. Alternatively, an electronic file may be created to map the good and bad die. The map is used to aide in the sorting process during the assembly operation.

3.2.9 Backgrind

In the fab, wafers are usually between 400-700 μm (15-30 mils) thick to provide enough mechanical support for the wafer during process. However, the chip separation

process works much better with thinner wafers. Thinner wafers may also be required for the packaged device, and can aide in the transfer of heat away from the device in the packaged product. For this reason, wafers are often thinned using an appropriate operation (backgrinding). Backgrinding is conceptually analogous to sanding; however it is much more delicate. In the backgrind operation, diamond cup wheels are used to grind the wafer to the required thickness. Final wafer thickness may range from 5-15 mils depending upon application.

3.3 Summary

Wafer fab processing includes may process steps: surface cleaning, epitaxy, oxidation, impurity diffusion or implantation, photolithography, etching, layer deposition, multiprobe, and backgrinding. It is important to have a fair knowledge of the complexity of the process in order to grasp the following concept. Various manufacturers supply the equipment used in wafer production. However, there is no standard on how the equipment interfaces with the wafer. As such, a large variety of end-effectors, motor drives, robot arms, and handling systems are used. *The only commonality between these transfer systems is the wafer. Therefore, it is important that the wafer itself be designed to withstand the process and support high process yield and, ultimately, profitability.* The next portion of this discourse will focus on the mechanical properties of materials, and the factors affecting their strength.

CHAPTER 4: MATERIAL MECHANICS

Understanding material mechanics will lead to meaningful consideration of a material's performance when subjected to external forces. Characteristics such as microstructure[7], mechanical shape, residual stress[8], thermal and mechanical history, etc. can all affect the structural integrity of a material.

Understanding the mechanical properties of a material is useful in design, so that the structural limitations of that material will not surprise the designer. Therefore, in order to make wise material selection decisions in the design phase, it is fundamental to have an understanding of the terminology, theory, and knowledge of a few test methods for material mechanical behavior.

A limited degree of material failure analysis skills may also be required in cases when the material uncharacteristically fails; these skills can lead to information about the material being tested, particularly if the material is new. Broek provides a summary of some of these techniques.[9]

4.1 General Mechanics[10]

Just as every action has an equal and opposite reaction, so when an external load is applied to a material, the material deforms due to slight changes in the atomic spacing. Stress σ is the term used for the external load and is usually given in units of pressure. The subsequent deformation or strain ε is defined as a percent equal to the change in length over the initial length.

The strain a material exhibits depends on a number of factors: atomic bond strength, stress, and temperature. Elastic deformation refers to reversible strain, or the ability of a material to return to its original state when the stress is removed. For tensile stress, Equation 4.1 defines this relationship; E is Young's modulus.

$$\sigma = E\varepsilon \tag{4.1}$$

For shear loading, Equation 4.2 defines the stress-strain relation ship

$$\tau = G\gamma \tag{4.2}$$

τ is the shear stress; γ is the shear strain; and G is the shear modulus.

A few material responses to tensile strain are shown below. Figure 4.1 shows brittle fracture, where the material behaves elastically with no plastic deformation up to fracture. Most ceramics and crystalline silicon behave in this manner at low temperatures. This response is typical at ambient and short-term loading, and is a critical characteristic to consider in design for structural purposes.

Many high purity crystals, including silicon, behave in this manner unless there is a suitable method for stress relief (e.g., generation of dislocations and dislocation movement at stresses lower than fracture strength).[11] If not, a crack front propagates along a crystal plane with relative ease. There is no means to relieve the stress and prevent the failure. A less catastrophic material response is crystal slip. Although the mechanism that causes crystal planes to slip past one another is still deleterious to semiconductor device physics, the material may not mechanically fail.

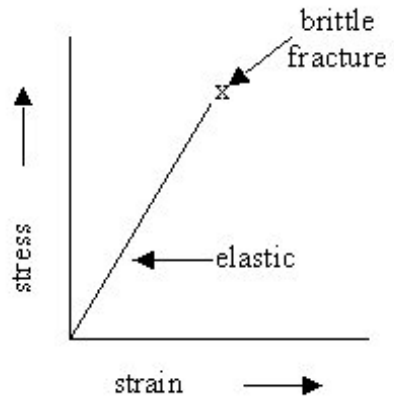


Figure 4.1: The stress-strain relationship for brittle fracture

Figure 4.2 shows plastic deformation with no distinct yield point. The material behaves elastically up to a certain stress, but instead of fracturing it deforms in a ductile manner as the stress increases. This deformation is referred to as plastic deformation or strain, and it is not reversible. Many metals exhibit plastic deformation.

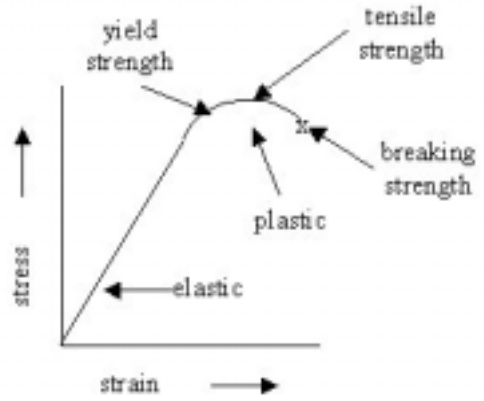


Figure 4.2: The stress-strain relationship for plastic deformation with no yield point

Other metals show plastic deformation with a yield point, a distinct discontinuity at the beginning of plastic strain. Figure 4.3 provides an illustration of this phenomenon. At high temperatures (600-1000^{o}C) Fischer, et. al. have demonstrated that silicon has a yield point when stressed in the <110> direction.[12]

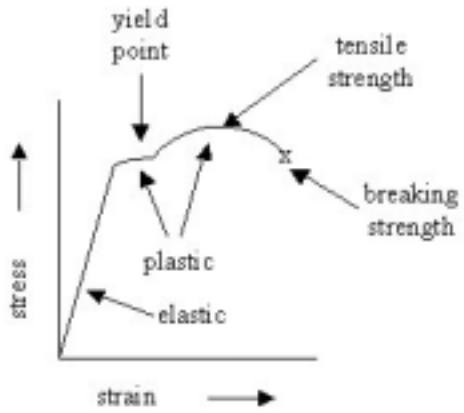


Figure 4.3: The stress-strain relationship for plastic deformation with a yield point

By rearranging Equation 4.1, the modulus of elasticity is defined:

$$E = \frac{\sigma}{\varepsilon} \tag{4.3}$$

E is the amount of stress required to produce elastic strain, and the magnitude of the elastic modulus is determined by the atomic bond strength in the material. Higher atomic bond strength means a higher elastic modulus. *E* may also vary in different crystallographic directions due to atomic packing density; closer packing results in higher bond strength. This anisotropy must be considered when dealing with single crystals like silicon. For polycrystalline materials, the elastic modulus is an average of all the crystal orientations in the sample. For amorphous solids, the modulus of elasticity needs no such consideration. Finally, the modulus decreases slightly with temperature because of thermal expansion, resulting in larger interatomic spacing. As the spacing increases, less force is required to further separate the atoms.

4.2 Fracture Mechanics

Fracture mechanics deal with strength and fracture in terms of crack surface displacement and the stresses at the crack tip. Stress intensity factors K_I, K_{II}, and K_{III}, are used to denote the stress concentration at a crack tip. The subscript refers to the mode, or direction, of the load applied with respect to the position of the crack. Mode I, represented by K_I, is used to describe a load that is perpendicular to the crack. This is the case with crack-opening or tensile and bend tests. Mode II, denoted K_{II}, describes sliding or in-plane shear loading; here the crack surfaces slide over one another in the direction perpendicular to the leading crack edge. Mode III, also K_{III}, involves tearing or the antiplane shear mode. In this case, the crack surfaces move relative to one another, and parallel to the leading crack edge. Figure 4.4 shows the various stress displacement nodes.

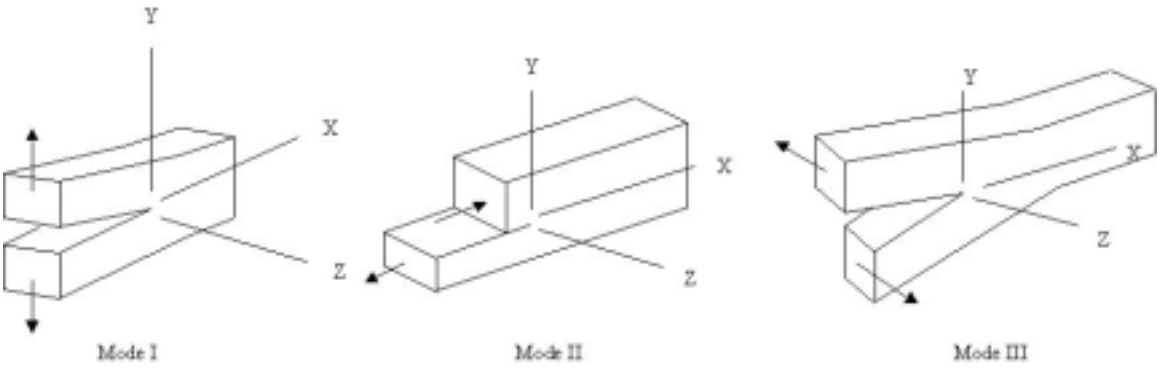


Figure 4.4: Modes of loading for different crack displacements

A large amount of attention has been given to mode I loading because of the general abundance of these situations in engineering applications. Most often the mode I critical stress intensity factor, or K_{Ic}, is characterized for a material. This is the stress intensity factor at which the crack will grow and lead to fracture, also called fracture

toughness. Higher fracture toughness means greater difficulty in initiating and propagating a crack.

4.3 Material Strength Testing

A material's resistance to deformation characterizes its strength. However, there are many factors that can be used to describe strength; theoretical strength, tensile strength, compressive strength, bend strength, and biaxial strength are all modifiers that can be used on the word "strength." This section will attempt to briefly outline the types of strength that exist, and how or if they are each tested.

4.3.1 Theoretical strength

One can define theoretical strength as the stress required to break atomic bonds. Equation 4.7 has been derived for estimating theoretical strength under tensile loads

$$\sigma_{th} = \left(\frac{E\gamma}{a_o} \right)^{1/2} \tag{4.7}$$

Where σ_{th} is the theoretical strength, E is the elastic modulus, γ is the fracture surface energy, and a_o is the interatomic spacing.

The presence of a defect such as a crack, pore, or inclusion results in stress concentration. Inglis[13] showed that applied stress σ_a was magnified at the ends of an elliptical crack in a non-ductile material so that

$$\frac{\sigma_m}{\sigma_a} = 2\left(\frac{c}{\rho} \right)^{1/2} \tag{4.8}$$

where σ_m is the maximum stress at the crack tip, *2c* is the length of the major axis of the crack, and ρ is the radius of the crack tip.

To demonstrate the stress concentration concept, one can assume that a crack tip is approximately equal to atomic spacing a_o (~2 Å). From Evans and Langdon, using a flaw size *c* of 170μm for reaction-bonded Si_3N_4 where fracture occurred at 150MPa, a stress concentration factor of 1840 is obtained by substituting into Equation 4.8.[14] Clearly, even a small flaw can be extremely critical and lead to substantial stress concentration.

4.3.2 Tensile strength

Ductile materials are usually tested for tensile strength, defined as the maximum load *P* divided by the cross-sectional area *A* (Equation 4.9):

$$\sigma_t = \frac{P}{A} \tag{4.9}$$

Testing can be accomplished a number of ways; uniaxial, hydrostatic, and theta tests are methods that are commonly used.

4.3.3 Compressive strength

Testing the crushing strength of a material gives that material's compressive strength. This method is especially useful for determining the usefulness of structural and load-bearing materials. Vickers and Knoop indentation tests, commonly used for hardness testing, have been correlated to the compressive strength of a material.[15] Indentation testers can take one of three approaches: direct, indirect, and modified.[16]

In the direct approach, a load *P* is applied to a sample via a pointed indenter. An indent with a diagonal length *2a* and radial cracks of total length *2c* are produced. The material hardness *H* is given by

$$H = \frac{P}{\alpha a^2} \tag{4.10}$$

where α is a numerical factor that depends on the shape of the indenter ($\alpha = 2$ for Vickers indenter).

By assuming that the stress intensity of the applied load is equal to the critical stress intensity factor for crack propagation, the critical stress intensity factor is obtained. Equation 4.11 gives the result.

$$K_{Ic} = \frac{\xi (E/H)^{1/2} P}{c^{3/2}} \tag{4.11}$$

H is the hardness determined by the load *P* and ξ is a dimensionless constant provided by the literature.

In the indirect approach, the strength of the material is measured after indentation, usually through bending techniques. Equation 4.12 gives the relationship between the K_{Ic} and the applied load.

$$K_{Ic} = \eta (E/H)^{1/8} \left(\sigma_m P^{1/3}\right)^{3/4} \tag{4.12}$$

Here σ_m is the strength, and η has been determined to be 0.59 +/- 0.12.

The modified form combines aspects of the direct and indirect methods. Here the sample is broken like in the indirect method, but there are typically multiple indents in the specimen before stressing. With this method the maximum crack length just before

failure can be measured from one of the other indents, and K_{Ic} can be determined from these measurements.

4.3.4 Bend strength

Brittle materials are commonly tested using bend strength tests. Samples may be circular, square or rectangular; this promotes easier and less expensive sample fabrication than specimens tested in tension.

For bending tests, the sample is supported at each end, and a load is applied at either one central point (3-point bending) or two points (4-point bending). The bend strength is defined by the modulus of rupture (MOR), or the maximum tensile stress at material failure. Equation 4.13 gives the bend strength of a rectangular structure

$$S = \frac{Mc}{I} \tag{4.13}$$

where M is the moment, c is the distance from the neutral axis to the tensile surface, and I is the moment of inertia. For a rectangular sample, $I = bd^3/12$ and $c = d/2$ where d is the thickness of the sample and b is the width. M, equal to the load P at one of the fixed ends of the specimen multiplied by the distance of the load away from the fixed end, varies with testing configuration. For three-point bending experiments, $M = (L/2) * (P/2)$ (Figure 4.5a). For four-point bending experiments, $M = (P/2) * a$ (Figure 4.5b).

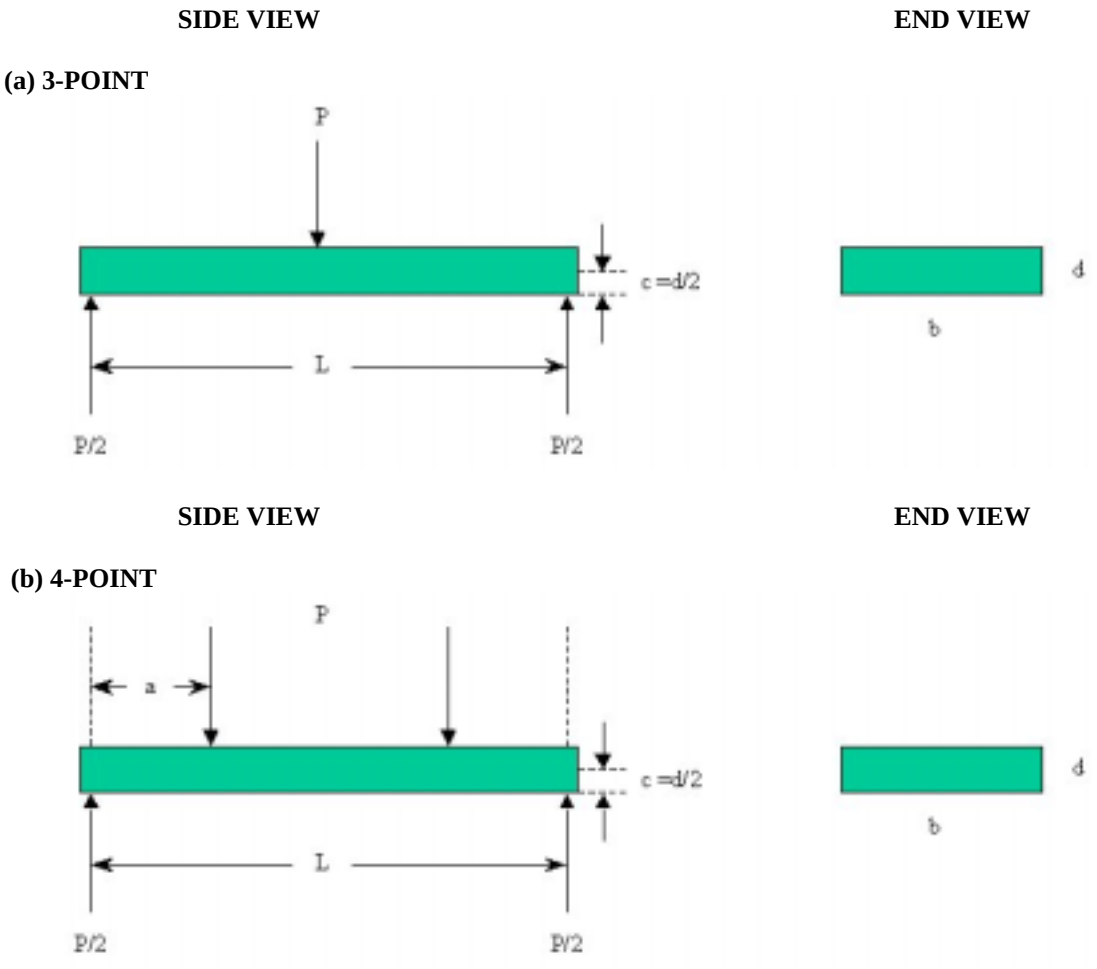


Figure 4.5: Geometry used to calculate the modulus of rupture. (a) For three-point bending, and (b) for four-point bending.

Caution is required when comparing data between tests. Since four point bending tests distribute the peak bending moment over a larger area (Figure 4.6),

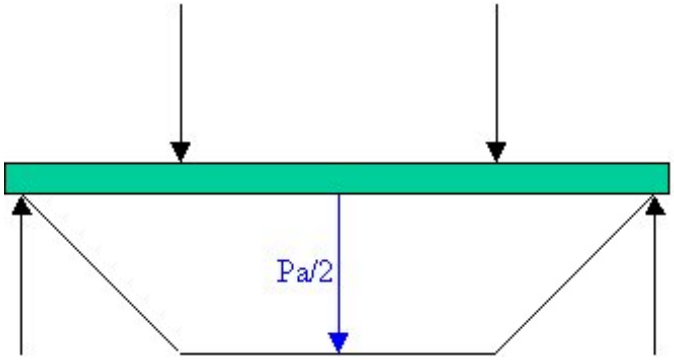


Figure 4.6: 4-point bending moment (blue arrows) and load points (black arrows)

The probability of a larger flaw being exposed to high stress is greater than with three-point bending (Figure 4.7).

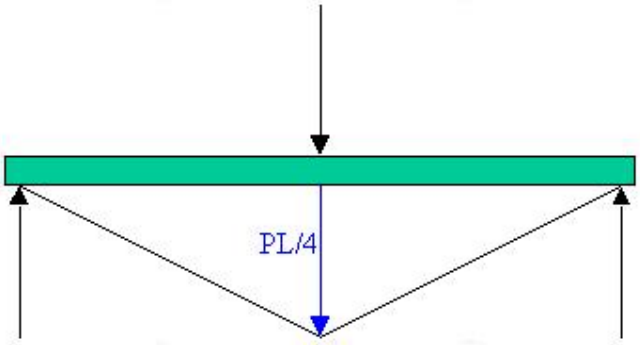


Figure 4.7: 3-point bending moment (blue arrows) and load points (black arrows)

For the same reason, uniaxial tests provide lower strength values for a given material than do bend tests (Figure 4.8).

Figure 4.8: Uniaxial stress distribution (blue area) and load points (arrows)

Horizontal shear stresses exist in bending beams, and this will be demonstrated below. Two equal rectangular bars with height *h* are placed on supports, and then a load *P* is applied (see Figure 4.9a). Without friction between them, each bar will bend

independent of the other as depicted in Figure 4.9b. Both bars will be in compression above the neutral axis and in tension below the neutral axis.

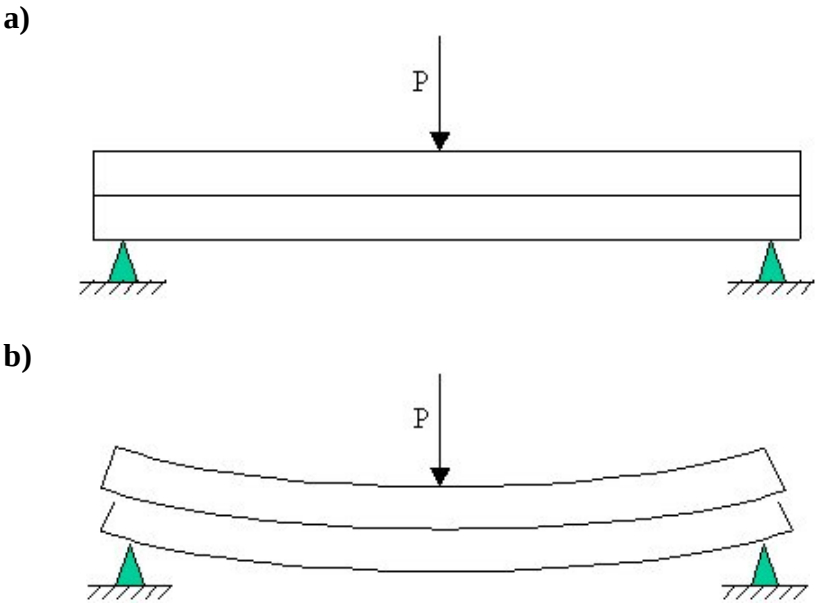


Figure 4.9: Bending of two separate bars

The lower surface of the upper bar will slide with respect to the upper surface of the lower bar. If this is a single bar of height *2h*, shear stresses must exist along the neutral axis to prevent sliding.

The cross section of the bar the rectangular beam has shear stress distribution as shown in Figure 4.10. The maximum shear stress τ_{max} is given by *3V/2A* where *V* is the shear force, and *A* is the cross-sectional area of the bending beam. For non-monolithic samples, failures like film delamination are adhesion failures due to shear stress. Bending tests that are conducted mid-plane, or on the neutral plane, are useful for film adhesion strength determination.

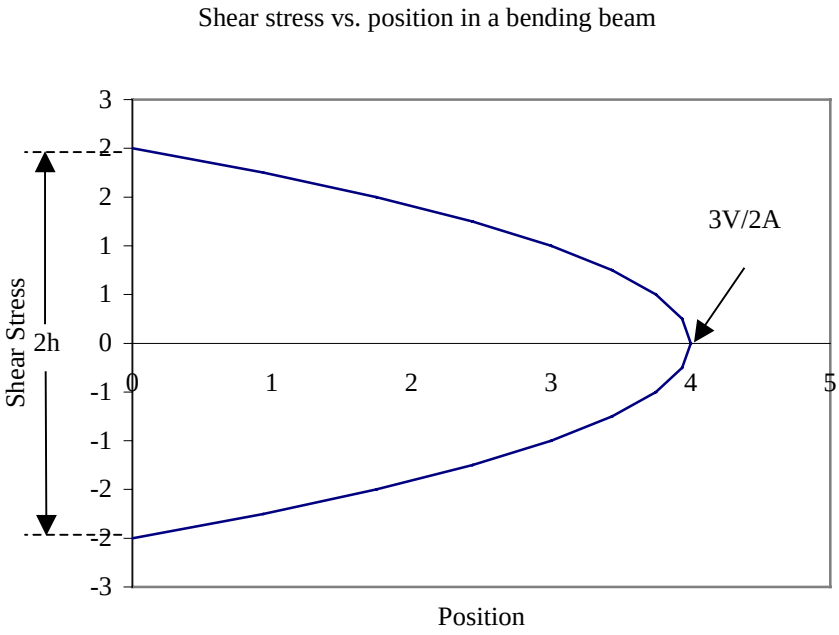


Figure 4.10: Shear stress distribution across a bending beam cross-section

To summarize, the observed strength of a material is dependent upon the type of test conducted and the flaw size distribution within the sample. As flaw size becomes more uniform, the strength values measured by different tests approach each other. For many materials, the apparent strength will decrease when going from three-point to four-point to tensile testing and as specimen size increases. Finally, shear stress is at a maximum in the mid-plane of a bending beam.

As mentioned earlier, if the sample is crystalline it is important to report the crystallographic orientation of the material with respect to the applied force. Silicon in particular has been reported to have K_{Ic} values dependent upon orientation.[17] One would expect this to be true for all materials with atomic packing densities that vary with respect to a fixed origin. That is, planes with higher atomic packing densities should be expected

to have lower interatomic distances, higher bond strength, and therefore higher K_{Ic} values.

4.3.5 Biaxial strength

The stresses discussed in the previous sections involve loading a material in a single axis, and are thus uniaxial stress mechanisms. However, there are many applications for materials that impose stresses in multiple axes. Unfortunately, few data are available for material responses to multiaxial stress fields. ASTM has a standard that applies to biaxial tests for ceramic substrates.[18] This standard has been used to characterize silicon wafers because of the brittle behavior similarity between ceramics and crystalline silicon; Bawa et. al. used the technique to suggest the preferred thickness of larger diameter wafers (i.e., >200mm). [19] The reader is referred to Richerson for additional discussion of biaxial strength.[20]

CHAPTER 5: FAILURE ANALYSIS OF WAFERS

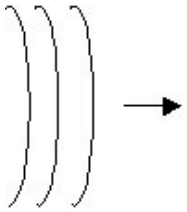
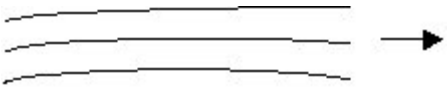
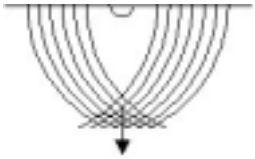
Even with the best material design considerations, situations can occur that may stress a material beyond its mechanical limits. In those cases, and especially when the root cause for failure is not immediately apparent, it is useful to perform failure analysis on the fractured surfaces.

5.1 Fracture Analysis

For brittle fracture there are often markings on the fractured edge that provide details about the origin, cause of fracture, speed of the crack at various locations, the orientation of the stress causing failure, and whether shear loading was present. The fractured edge inspection method is commonly used for ceramics and glasses.[21] However, it is not often used in the semiconductor industry even though similar markings appear on many semiconductor materials, as indicated by Dyer.[22] Using these markings, the cause of four different types of wafer breakage events were identified and fixed. Some of these markings appear below in Table 5.1.

The technique for fractured wafer edge inspection is described in other work.[23] The method is simple, and it involves little in the way of equipment; a low power stereomicroscope (7-30x) is usually all that is required. Finally, wafers with various crystallographic orientations can be analyzed with this technique, since the markings are a result of shear and stress relief in the material, not crystallography.

Table 5.1: Some fracture markings on semiconductor wafers

Marking Name	Appearance and Direction of Travel	Uses
Rib		Finding origin and direction of travel
Hackle		Finding origin and direction of travel
Wallner Lines		Finding origin

Rib marks are perhaps the easiest to see. They appear because the crack sometimes proceeds, not on a fixed crystal plane, but by oscillating back and forth around a plane to relieve the applied stress.[24] According to literature, oblique lighting or interference contrast sometimes aides in imaging. Figure 5.1 shows obvious rib markings on a silicon wafer using a low power stereoscope.

Hackle marks occur when the material tears on two different levels and must tear the step between them to advance. These marks are usually normal to the advancing crack front. Wallner lines are fine, rib-like markings where the crack front is intercepted by transverse shear waves; obstacles snagging the surface of the wafer usually produce these lines. These lines are most helpful in determining the origin of the crack.

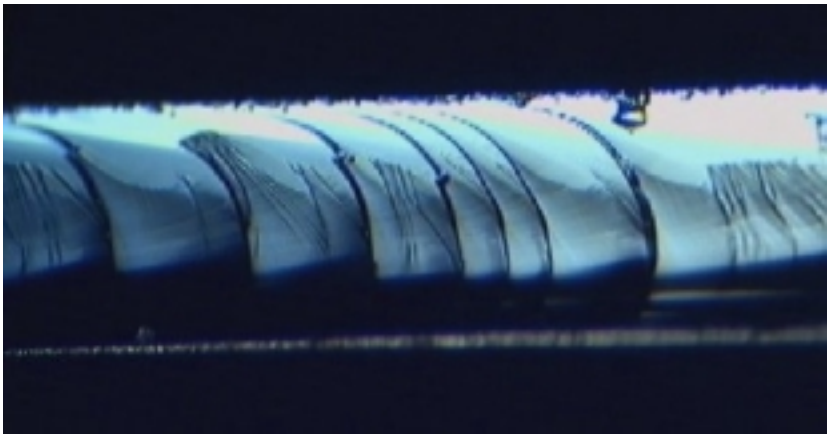


Figure 5.1: Rib markings on a silicon wafer

While used very little in the semiconductor industry, the fracture tracing technique may someday become much more largely accepted as the cost impact of a fractured wafer rises with technology advances and increases in wafer diameter.[25] Certainly, the tool is useful in providing crucial information about the circumstances of the wafer failure, and is another instrument to be used by engineers in improving process conditions.

5.2 Using Fracture Analysis to Identify Potential Problems

Understanding that a fractured wafer edge may yield information about the origin of fracture is one thing, but using this information to solve a problem is another. The following method may be useful to provide a guide on how to determine the root cause of wafer breakage events in wafer fab processing.

5.2.1 Determine the fracture origin

The first step is to determine the origin of the wafer fracture. Using simple equipment like a stereoscope, the fractured wafer edge is viewed. One should look for

characteristic markings like those depicted in Table 5.1. Once a discernable pattern is found, it should be traced to the origin. The origin may be determined by looking for places where the wafer is discolored (signaling oxidation of a fractured surface), where multiple crack lines converge, or where there are obvious signs of silicon smashing.

5.2.2 Record the location of the origin

In the next step, the location of the origin is recorded using a suitable frame of reference. It may be helpful to radially partition the wafer into sizable zones to help in this analysis. Table 5.2 provides an example of how a wafer may be divided into zones. Figure 5.2 is a graphic illustration of Table 5.2.

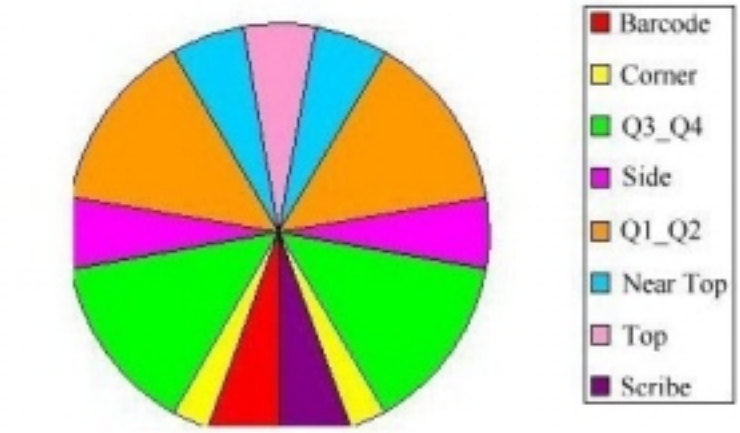
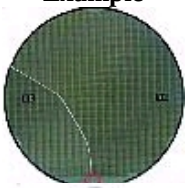
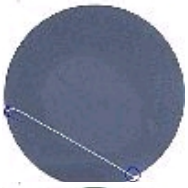
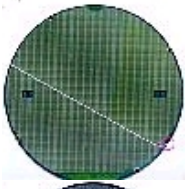
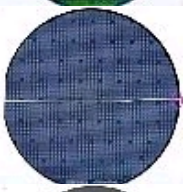
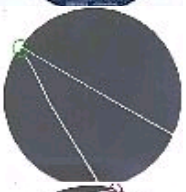
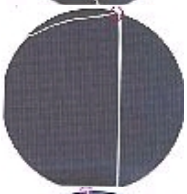
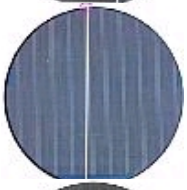
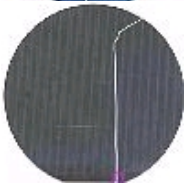


Figure 5.2: Wafer Breakage Zones

Table 5.2: Wafer locations with the flat down

Location	Significance	Example
Barcode	Laser etched barcode at the bottom portion of the wafer near the flat	
Corner	Where the orienting flat meets the rounded edge	
Q3_Q4	Third and forth quadrants of the wafer	
Side	The left or right sections of the wafer	
Q1_Q2	First and second quadrants of the wafer	
Near Top	Portions of the wafer to the immediate left or right of the top	
Top	Top of the wafer	
Scribe	Optical character readable (OCR) laser scribe etched near the flat	

Now it is possible to classify the different types of breakage events according to the origin at the wafer edge. For example, using Figure 5.2 and Table 5.1, a wafer whose breakage origin in the first quadrant would be classified as "Q1_Q2." If you assume that wafer breakage is the result of equipment interactions with a wafer, the next logical step is identify various types of equipment that contact the wafer in each zone.

5.2.3 Build a wafer breakage database

The process can stop here if the user intends to solve only single wafer breakage events. However, if the user intends to catalog and identify problems over time, it is helpful to record all pertinent information about the breakage event into a database. In this manner, problems that are perceived as low-level issues can be established in time as higher impact problems. The necessary resources will often be devoted to address the issue once enough data has been gathered.

This process, start to finish, takes limited equipment resources. However, since it may take a few minutes per wafer to identify and trace the fracture origin, time is a resource that is required to analyze many wafers. In the end, the potential pay-off is well worth the investment.

5.3 A Short Case Study of Fracture Analysis in Use

Using the technique and fracture origin frame of reference outlined above, over 160 broken 125 mm wafers were collected for a period of two months at a TI wafer fab in Sherman, Texas in late 1999. Along with the origin of the fracture, the wafer orientation,

the equipment upon which the broken wafer was found, and the logpoint, or location in the process flow, were all recorded.

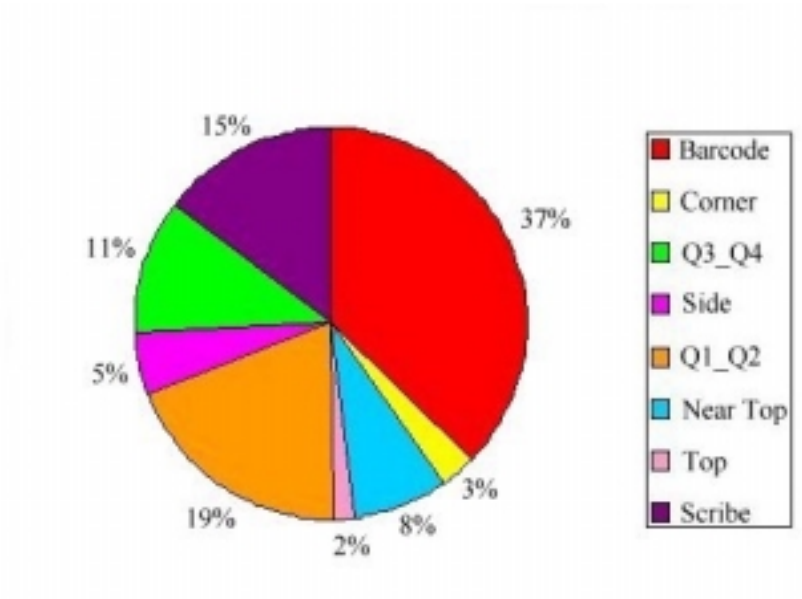


Figure 5.3: Observed Wafer Breakage Locations

After analyzing the data, a few conclusions were reached. First, nearly every wafer collected had its fracture origin at or near the wafer edge. This lead to the theory that a wafer's edge design is significant in determining the mechanical properties of the wafer in relationship to the process (more on this subject in Chapter 7). Next, by creating a histogram of breakage by origin at the wafer edge (see Figure 5.3), it is possible to see the frequency of breakage as a function of the zone in which the breakage occurred. Figure 5.3 indicates that nearly 37% of the wafers collected had a breakage origin in the barcode (more on this subject in Chapter 6).

Clearly, this study lead to very interesting and powerful information. Prior to this study, little was known about the magnitude of the breakage problems that were attributable to the edge or barcode design. The next two chapters will discuss how these

two pieces of information were used to address specific wafer design issues. Modifications to the present designs will be investigated as a means to reduce wafer breakage tendencies.

CHAPTER 6: THE EFFECT OF BARCODE DOT DENSITY AND CHEMICAL ETCHING ON SILICON WAFER MECHANICAL PROPERTIES

6.1 Introduction

The barcode is a 2.4 mm line of individual laser-scribed dots on the front surface of the wafer near the flat. Also located near the flat is a human readable optical character readable (OCR) alphanumeric character string. The barcode is the machine-readable OCR equivalent.

The barcode is used as an automatic method to verify that a wafer is in the correct location in the fab process. Furthermore, by scanning the barcode prior to processing, a fab's engineering group can gather information about the uniformity of a particular process. For example, if the exact position of all 200 wafers in a thermal furnace is known during a diffusion operation, it may be trivial to track the cause of a yield distribution within a particular lot to the position of the wafer within the furnace. (Furnace temperature zones can vary, and will affect yield if the drift is too far from the target value.)

In Chapter Five it was indicated that nearly 37% of all wafer fractures originated in the barcode region. Furthermore, almost all of the wafers analyzed had breaks that originated in the barcode. That is, only a very small percentage of breaks occurred in the barcode region, but did not originate in the barcode.

A schematic of the barcode and OCR locations near the wafer flat appears below in Figure 6.1.

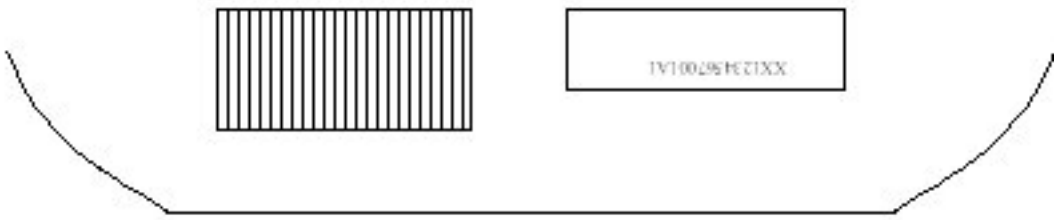
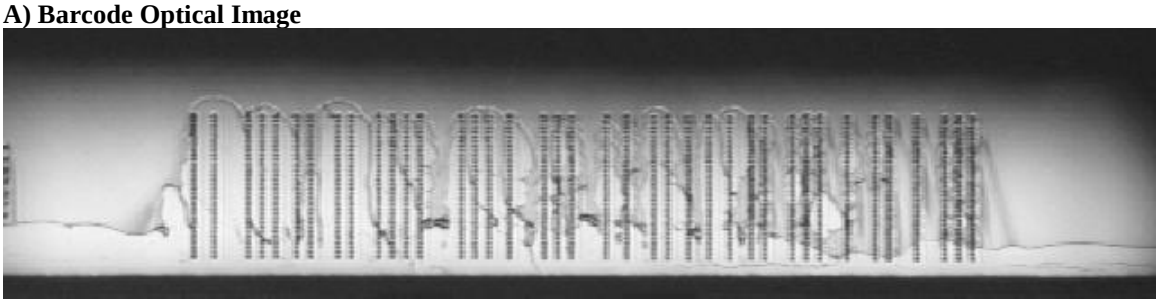


Figure 6.1: Schematic showing approximate barcode and OCR locations on a wafer. The barcode is on the left; the OCR is on the right.

Figure 6.2a and 6.2b shows optical photographs of a barcode and OCR laserscribe, respectively.

A) Barcode Optical Image



B) OCR Optical Image

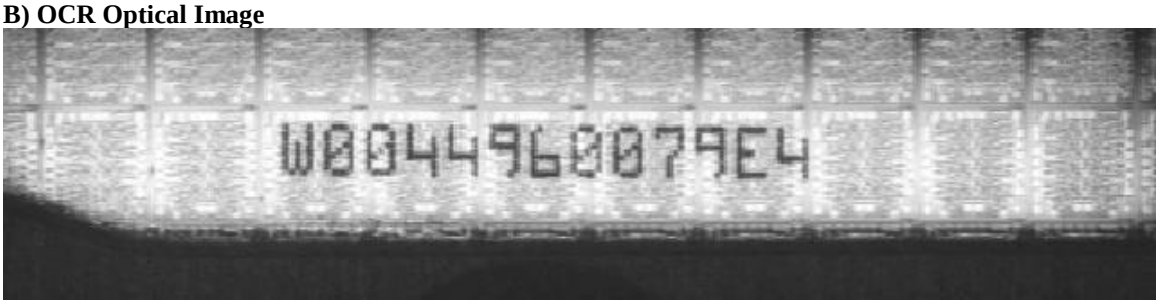
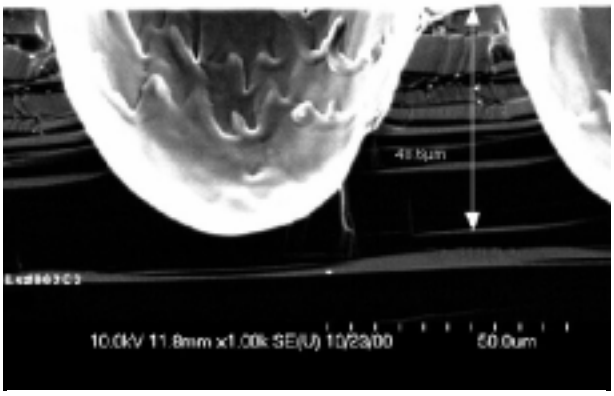


Figure 6.2: Examples of barcode and OCR laser markings on wafers

Different manufacturers may use different dot densities even when supplying material to the same specification. (Barcode dot density was an unspecified parameter.) Comparing suppliers, one can find one supplier using a dot density of 9.17 dots/mm while another using a dot density of 12.5 dots/mm. Further, the study also revealed that

suppliers may use an isotropic or anisotropic etch during wafer manufacturing sometime after the dot is scribed on the wafer. (The reader is referenced to discussion of ODE etching in Chapter 3 for more information on anisotropic etching.) The difference in configuration between the manufacturers caused a series of tests to determine how barcode dot density and chemical etching might affect the mechanical strength of a wafer near the barcode region of the wafer. The theory that stress concentration could be occurring at the barcode was investigated through a modification of three-point bending tests (more on this below). Figure 6.3 shows two individual cross-sectioned dots from a wafer barcode.

A) Isotropic Profile



B) Anisotripic Profile

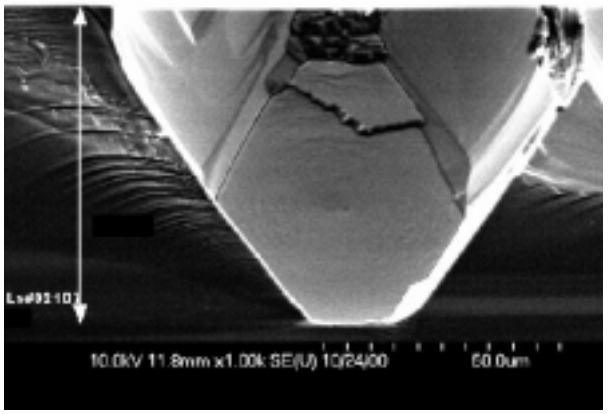


Figure 6.3: SEM image for the difference in cross-sectional profile of barcode dots that have been etched a) isotropically and b) anisotropically.

A design of experiment (DOE) was developed to investigate these effects; each "leg" had a different configuration. The DOE appears below in Table 6.1. Because of the manufacturing flow at the supplier, wafers are scribed to an initial depth prior to lapping and polishing the surface of the wafer. Thus, the final depth of the laser scribe is not established until after the wafer surface is polished. This depth may vary depending upon whether the wafer is reworked or not. Table 6.1 notes the approximate final depth of the dot scribe as determined by SEM cross-sections. The DOE wafers were 125 mm in diameter and 15 mils thick.

Table 6.1: Wafer test matrix

Wafer Type	Number of Dots	Etch	Approximate Final Scribe Depth (μm)
Baseline	30	Anisotropic	80
DOE 1	22	Anisotropic	80
DOE 2	22	Anisotropic	60
DOE 3	22	Anisotropic	50
DOE 4	22	Isotropic	50

6.2 Wafer Barcode Dot Density Experimental Method

To test the wafer at the flat, a modification of the notched-sample three-point bend test was used. In the test rig a wafer was fixed face down on a Styrofoam cushion with the barcode facing the cushion. An IMADA motorized test stand (MV-100) with a digital force meter (DPS-110R) was used to measure the peak force to fracture a wafer through the barcode. A pointed stylus was affixed to the end of the force meter and lowered by the test stand onto the backside of the wafer corresponding to the barcode region. The tests were used to compare the performance of the DOE wafers against each other. At least three wafers were tested from each group.

6.3 Barcode Dot Density Results and Discussion

The results of the barcode dot density tests appear below in Figure 6.4. The average force to fracture wafers in the barcode region are reported for each type of wafer tested.

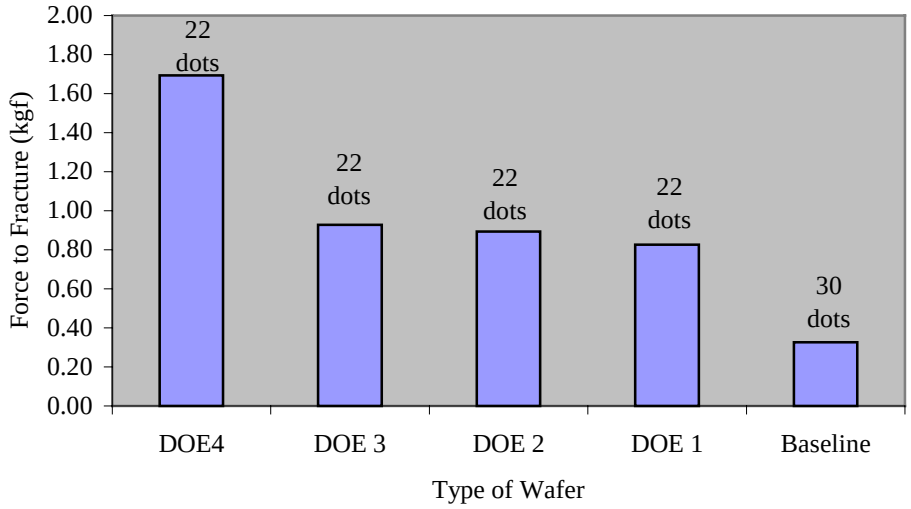


Figure 6.4: Dot Density Test Results

The results of the breakage tests are summarized in Table 6.2.

Table 6.2: Breakage Test Results

Wafer Type	Ave Force to Fracture (kg_f)	Standard Deviation (kg_f)
Baseline	0.33	0.01
DOE 1	0.83	0.14
DOE 2	0.89	0.33
DOE 3	0.93	0.11
DOE 4	1.69	0.26

The breakage strength of a 125mm wafer in a region with no barcode was also tested to compare the regions with and without barcode. The results are compared with

the DOE values, and they appear in Figure 6.5. The average force to fracture the wafer in a non-barcode region of the wafer was 6.03 kgf with a standard deviation of 2.08 kgf.

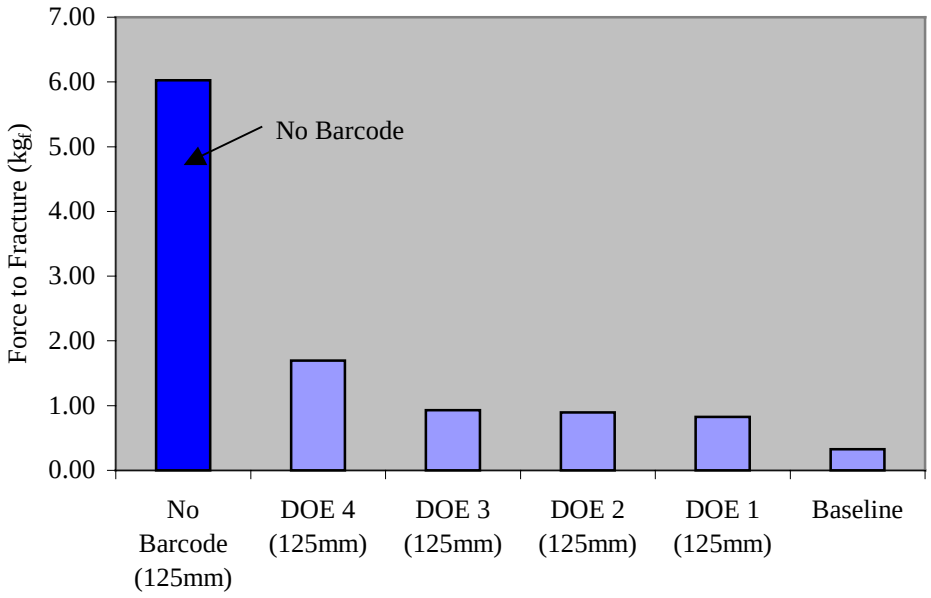


Figure 6.5: Dot density test results compared to wafer with no barcode

The data indicate that wafer strength increased by roughly 250% with about a 30% reduction in dot density for 125mm wafers. The data also shows that dot depth of the barcode has much less to do with the strength than dot density. The effect of the ODE etch on the wafers appears to be the main cause for the difference in mechanical performance between test groups.

6.4 Conclusions

After considering the data, it is believed that the ODE exposes the crystal plane, and allows for forces to be focused along this geometry. Chapter 4 discussed brittle fracture of crystals in terms of stress relief. Since highly pure crystal silicon does not

have a suitable means to relieve stress, fracture often leads to material failure. The combination of the ODE and the dot density creates a higher stress concentration in the product.

In summary, the barcoded silicon wafer is not as strong as the uncoded silicon wafer. A wafer tested in the non-barcode region is about three times stronger than a wafer tested at the barcode. ODE wafers expose crystal planes (see Figure 6.3), and this enhances a wafer's potential to fracture. The effect of the depth of the laser dot is not as important as the density or the etch process used in manufacturing the wafer.

CHAPTER 7: THE EFFECT OF WAFER EDGE DESIGN ON SILICON WAFER MECHANICAL PROPERTIES

7.1 Introduction

In the semiconductor industry, there are certain entities that were created standardize specifications and methods. One of these organizations is Semiconductor Equipment and Materials International (SEMI). SEMI has created a number of international standards for the purpose of standardization. One of their standards, SEMI M1, focuses on wafer edge bevel profiles. Figure 7.1 shows the SEMI M1 standard T/3 window for 125mm wafers. (T/3 denotes thickness divided by three; a subset of M1 also specifies characteristics for T/4.) Each wafer diameter has its own specification for the A, B, C, and D dimension in Figure 7.1.

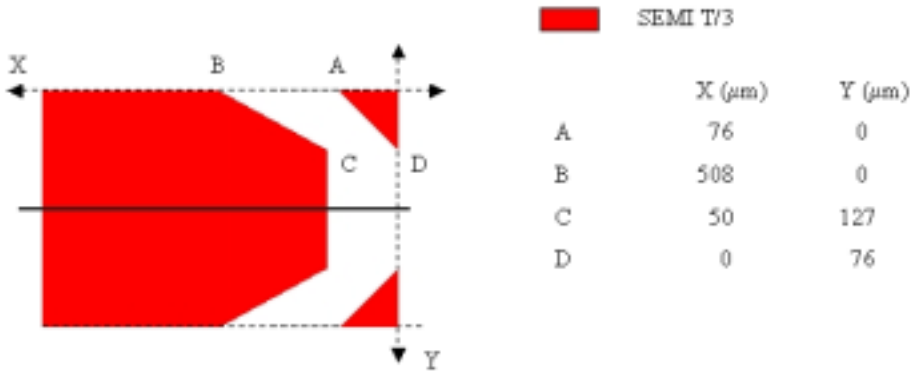


Figure 7.1: SEMI M1, the T/3 standard for 125mm wafer dimensions – the wafer edge profile must fall within the white area; the red zone is forbidden.

To test the edge bevel, an experiment was designed to vary the wafer bevel length (either 500, 800, or 575 microns) and radius of curvature (either 0.05 or 0.17 mm). The baseline product was a 125 mm wafer, 15 mils thick with a 500-µm bevel length *L* and

0.05 mm radius *R*. A wafer manufacturer provided the test wafers. Figure 7.2 depicts the edge bevel characteristics and nomenclature.

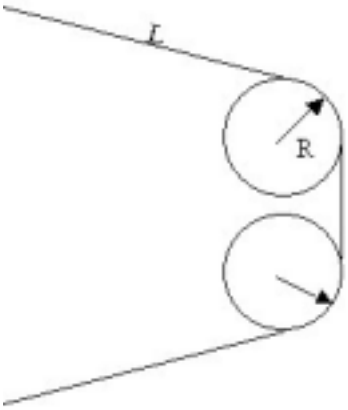


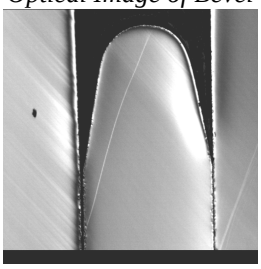
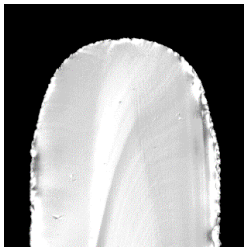
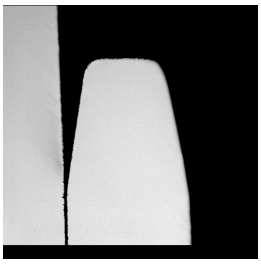
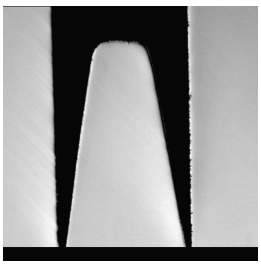
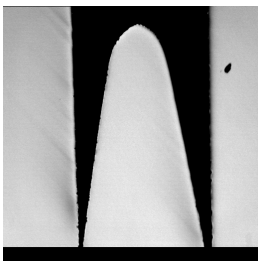
Figure 7.2: Characteristic dimensions of a wafer edge bevel: length *L* and radius *R*. A bevel 500 um long with a 0.05 mm radius is denoted 500R0.05.

Table 7.1 tabulates the pertinent information from the edge bevel design of experiment (DOE). Included are the type of wafer, physical dimensions of the beveled edge, and an optical image of the bevel.

7.2 Mechanical Edge Tests Experimental Method

Two separate tests were used to evaluate the wafer edge design. The first, a drop test, allows one to evaluate the edge integrity when the force is applied normal to the wafer edge. The test involved dropping the wafer from a nominal height of 10 cm through a guided post onto a hard surface. Figure 7.3 shows a schematic representation of the drop test.

Table 7.1: Edge Bevel DOE Characteristics

Wafer Type	*Bevel Length (μm)*	*Bevel Radius (mm)*	*Optical Image of Bevel*
575R0.17	575	0.17	
500R0.17	500	0.17	
500R0.05	500	0.05	
800R0.05	800	0.05	
800R0.17	800	0.17	

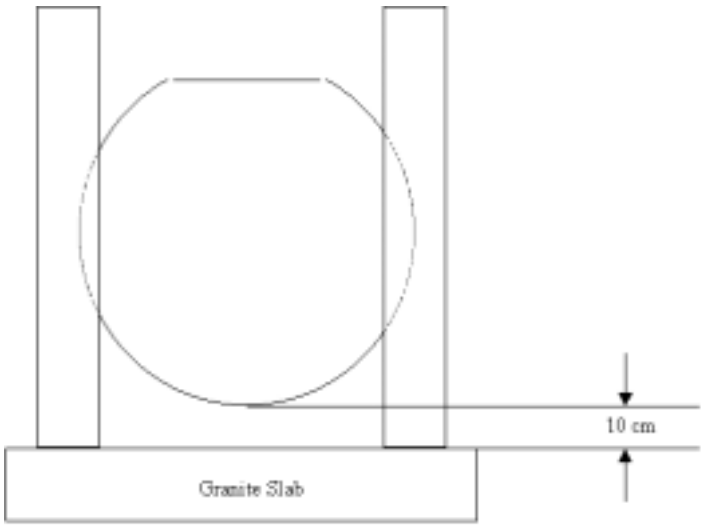


Figure 7.3: Schematic Representation of the Drop Test

The second test, an edge chipper, tests applied force at a different angle. The edge chipper consisted of a spring-mounted weight anchored to a base-plate. The weight was pulled back a fixed distance and released to strike the wafer. A schematic representation of the strike test is shown in Figure 7.4. For either test, the number of iterations was counted until the wafer either broke, chipped, or fractured (BCF). A few wafers were tested using each technique.

Two separate tests were chosen to evaluate the performance of the edge bevels in an effort to try to simulate the forces that might be exerted upon the wafer during processing. For instance, the drop test approximates the stresses on a wafer due to an operator dropping the wafer into a cassette (a carrier for the wafer in the fab), or the load on a wafer standing on end in a furnace operation. The strike test simulates the interaction a wafer might have with a robot arm or mechanical fixture in a machine during processing. Between the two tests, it was figured that the best design would reveal itself.

Figure 7.4: Schematic Representation of the Strike Test

7.3 Wafer Edge Test Results and Discussion

The results of the edge bevel drop tests are presented below in Table 7.2 and graphically in Figure 7.6.

Table 7.2: Results of the Drop Tests

Wafer Type	*Bevel Length (μm)*	*Radius (μm)*	*Ave. Drops to Fracture*	*Std Dev*
575R0.17	575	0.17	>410.0	52.0
500R0.17	500	0.17	183.0	94.1
500R0.05	500	0.05	114.7	86.3
800R0.05	800	0.05	8.3	5.1
800R0.17	800	0.17	1.7	1.2

Clearly, the 575R0.17 edge design performed much better than the other bevel designs. In two of the three samples, the wafer did not break, chip, or fracture even though the wafer had been dropped 440 times. The next best performing design was the 500R0.17. Though the two bevels appear similar, there is enough difference in the 575R0.17 and 500R0.17 edge profiles to be measured in the drop tests. Closer inspection reveals that the 575R0.17 has a slightly more uniform profile than the 500R0.17.

A typical edge chip appears in Figure 7.5; the chip in this figure is about 0.5 mm large.

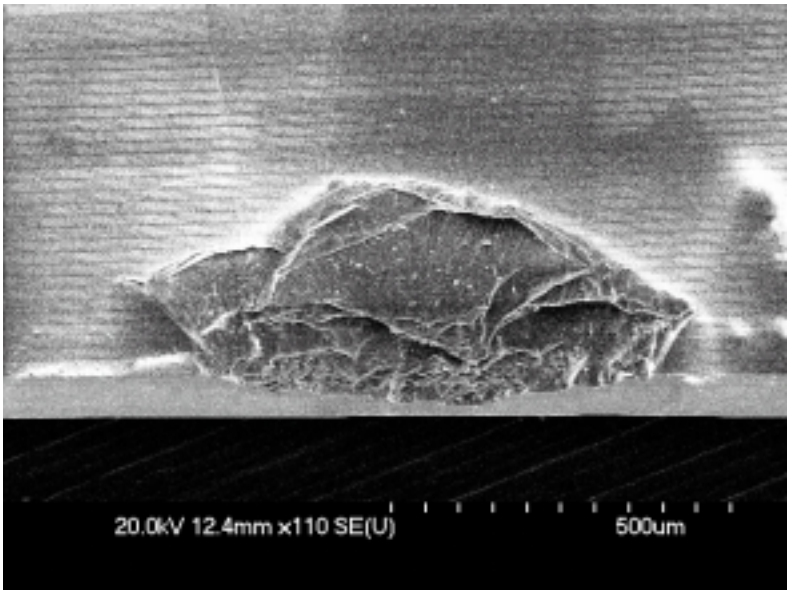


Figure 7.5: SEM image of a typical edge chip after drop test.

The results of the wafer edge strike tests can be seen in Figure 7.7. As in the drop test, the 575R0.17 bevel design performed much better than the remaining designs. However, in these series of tests, the 800RXX (XX = 0.05 or 0.17) wafers performed better than the 500RXX ones. The cause for the change in performance may be due to bending of the more pointed tips. Since there is less silicon mass at the end of the 800RXX profiles, there could be a tendency for the silicon to flex slightly, certainly more than it might in the 500RXX configurations. Failures in the strike test were also much more catastrophic than in the drop tests. Many wafers shattered upon failure.

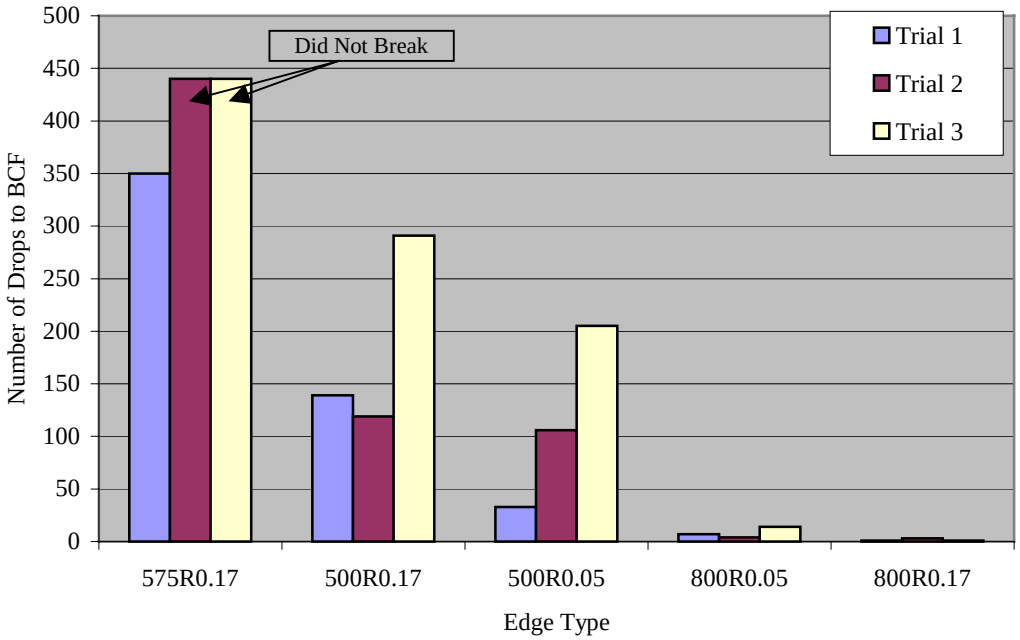


Figure 7.6: Results of the Drop Test

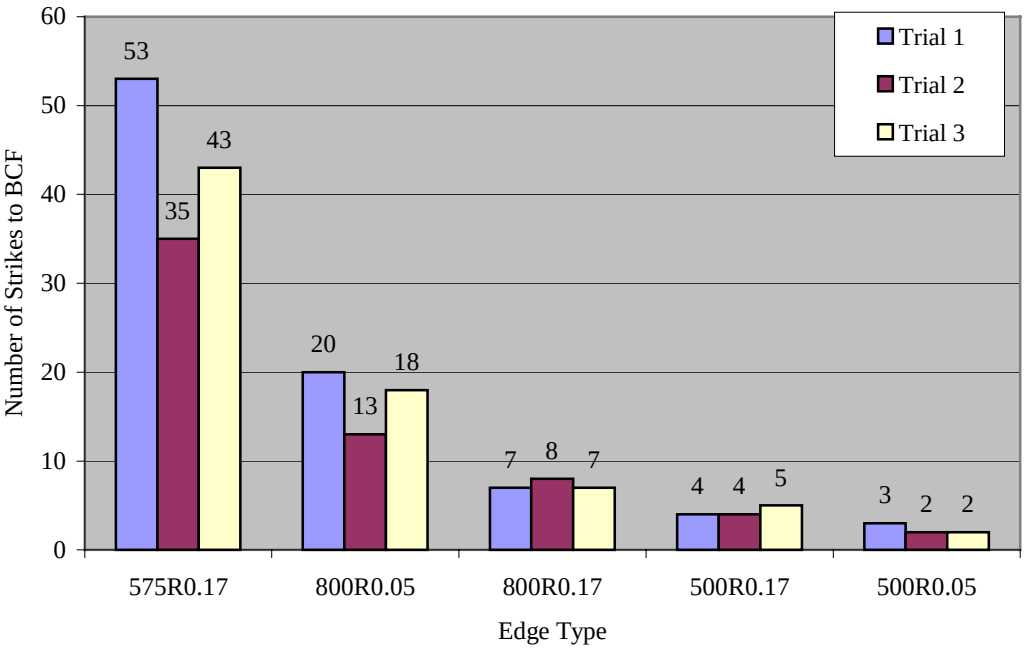


Figure 7.7: Results of the Strike Test

Various silicon wafer manufacturers have initiated numerous US patents on methods to bevel wafers. Clearly, there is a reason so many companies have invested the time and effort into patenting the various beveling means and profiles. At least one patent claims that edge chipping will be reduced because of the bevel profile.[26] However, the literature does not indicate how the bevel profile affects the distribution of force upon impact.

If one looks to classical mechanical designs for guidance, a hint of the underlying force distribution principle can be seen. It is then a trivial matter to extend this application to silicon wafers. Pre-Industrial Revolution structures were usually designed to be in compression because the materials of construction were often brittle (e.g., brick and mortar).[27] Figure 7.8 is a schematic of a Roman bridge in the shape of an arch. The arch shape causes loads to be transmitted through the structure as compressive stresses.

Now, a similar argument can be made for the edge bevel design. Silicon, also a brittle material, has poor mechanical properties in tension. However, by designing a beveled edge on a wafer, it may be possible to create compressive stresses when an external force is exerted upon it. Forces that may have resulted in catastrophic failure for an unbeveled edge, may now act to keep it together.

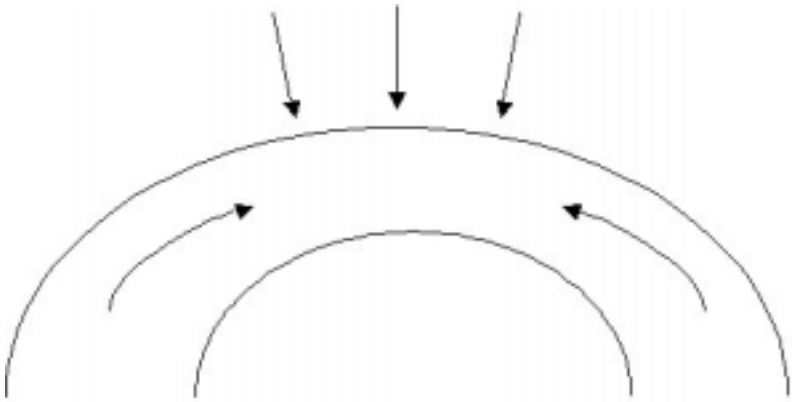


Figure 7.8: Schematic of a Roman bridge design. The arrows indicate forces acting on the bridge.

Further, it may be significant that the edge bevel that performed the best in both the drop and strike tests was also the one that had the smoothest edge design. That is, the edge profile did not drastically change along the bevel and into the radius. One might image the other bevel designs to contain "hot spots" at the locations where there is a distinct change in edge profile. These locations could be where applied forces would be very strong, thus leading to failure.

7.4 Conclusions

These tests indicate that wafer edge design is critical in the consideration of silicon wafer mechanical properties. The edge profile that performed the best in both the drop and strike tests was the one that had the most uniform shape throughout the bevel (i.e., no drastic change in profile from bevel length to bevel radius). In comparison, profiles that were markedly pointed or blunted generally performed worse than the other test groups. These wafers are considered to have forces concentrated at location(s) where the profile changes drastically. The concentrated force leads to chipping of the edge, and possibly wafer failure.

CHAPTER 8: CERAMIC COATINGS FOR MECHANICAL SUPPORT OF SILICON WAFERS

8.1 Coatings for Enhancing Mechanical Properties

Coatings are composite materials with a layered structure, usually consisting of two or more components.[28] Various types of coatings exist, but among the most utilized types are corrosion inhibitors and sacrificial layers (e.g. metallic or ceramic coated metals). Other types of coatings include organic materials (paints, lacquers, and thinners).

In the discussion of material testing, one particular area has been omitted. That is the concept of material strengthening. Depending upon the material, there are various strengthening methods that are used. For metals, the following practices are commonly used: alloying, work hardening, annealing, quench hardening, tempering, solution treatment, and precipitation hardening. Porter and Easterling provide information on the techniques used for metals.[29] For ceramics, another set of mechanisms exist: crack deflection, crack bowing, crack branching, and crack tip shielding by process zone activity or crack bridging. Wachtman summarizes modern ceramic toughening practices.[30] However, neither metal nor ceramic toughening techniques readily apply to crystalline silicon since the techniques usually involve modifying grain structure or incorporating a second precipitated phase. Each of these implies that the material must be polycrystalline in order to benefit; this excludes the silicon used in semiconductor manufacturing. Thus, any attempt to increase the mechanical properties of a silicon

wafer must ensure that crystallinity is maintained. For this reason, the use of ceramic coatings will be investigated.

The concept of coatings is not new, but the application to wafers as a structural component may be since the literature has not provided information about their use to improve mechanical properties. At this point, it is worthwhile to note that ceramics and crystalline silicon generally behave with some similarity; namely, both are brittle. This begs the question, "Why choose a brittle ceramic as a coating to improve the mechanical properties of brittle substrate?" The answer may not be so simple.

First, one should consider why a ceramic coating might work. A traditional mechanical toughening scheme for ceramics may involve second phases within the bulk material. The purpose of the second phase material (i.e., whisker-like fibers) is to distribute a load through the bulk of the material when stressed. If a crack propagates through the material and intersects the secondary phase whisker, the force of the crack will be distributed along the length of the whisker. If the whisker is pre-tensioned, then it may even act to close the crack front. While this is not an acceptable approach for silicon wafers, the toughening mechanism may be extended in a similar manner if a pre-stressed film is deposited upon the wafer. A compressive film may act in the same manner to close a crack front when the substrate is stressed beyond its typical limit. For this reason, films with various residual stresses will be tested.

8.2 Choice of Coatings

8.2.1 Silicon Dioxide[31]

Silicate glasses, comprised of SiO_2 as the glass former, are generally considered to typify brittle behavior as discussed in Section 4.1 of this chapter. Experiments indicate that glass with a "normal" surface usually fails at the surface due to significant flaws. If the glass can be prepared without these surface flaws, then very high strengths may be obtained. Kurkjian carefully prepared silica fibers with strengths as high as 14 GPa, or about *E/5*.[32]

Owing to the surface flaws, the strength of bulk glass is usually far below the theoretical strength (about two orders of magnitude). Flame or chemical polishing can accomplish flaw removal, but some glasses will degrade with the chemical or mechanical action. A more useful approach is to induce a compressive stress in the surface layer by thermal tempering, ion exchange, or other methods.[33] A summary of glass strengthening techniques appears below in Table 8.1.

Table 8.1: Various treatments to strengthen glass[31]

Treatment	**Approximate Strengthening Factor**
Quench hardening	6
Ion exchange	10
Surface crystallization	17
Ion exchange and surface crystallization	22
Etching	60
Fire polishing	200
Second-phase particles	2

Thermal tempering of glass is very unlike the process of tempering metals like steel. Instead of precipitating second phases, tempering glass involves the creation of compressive stress at or near the material surface. The compressive stress is balanced by

an internal tensile stress. Since glass failure usually involves the propagation of a flaw at the surface, any applied force at the surface of tempered glass must overcome the compressive stress nature of the surface before the crack can propagate.

Thermal tempering of glass is accomplished by bringing the temperature of the bulk glass above the annealing temperature. Holding this temperature for a sufficient time and then rapidly cooling the glass creates a thermal gradient within the solid. Initially, the surface drops below the annealing temperature while the center stays above it. The temperature continues to drop, and as it does the surface reaches room temperature. As the center continues to cool to room, it attempts to contract and pulls the surface into compression.

Chemical strengthening can produce greater strengthening, and may be divided into three types: compound glass, ion exchange, and surface crystallization. A compound glass contains surface layers of low thermal expansion upon a core of high thermal expansion. This can produce high compressive surface stresses, but the glass will suffer from edge effects. Ion exchange involves exposing the glass at high temperatures to ions that are larger than those originally present in the glass. Exchanging Li for Na, for example, has produced strength as high as 482 MPa. Strength in excess of 690 MPa can be produced by surface crystallization of a low expansion phase at high temperature.

8.2.2 Silicon Nitride[34]

Silicon nitride is generally considered the leading candidate for structural use above 1000^{o}C although silicon carbide is also used. Nitride has two structural forms, α and β; both forms are hexagonal. The α form is made up of alternating layers of β form

and its mirror image. The α form of nitride has nearly twice the *c* axis as the β form (*a* = 0.775 nm, *c* = 0.5168 nm for α; *a* = 0.07608 nm, *c* = 0.2911 nm for β). The α form is thought to exist only when kinetic forces predominate, and nitride powders are generally in the α form. The β form is thought to be the stable form, and solid specimens of nitride are generally in this form. The transformation from α to β takes place during sintering.

Solid nitrides made from powder generally contain a few percent of sintering additives, such as alumina or yttria. A small amount of silica may also be found due to oxidation or through deliberate addition. The sintering additives improve properties by allowing full or nearly full density and promoting elongated grain growth.[35] At high temperatures, though, the same additives increase the creep properties of nitride.[36] Thus, the performance of the nitride must be considered in conjunction with the expected stress and temperature of the application.

An alternative method to produce solid silicon nitride is forming a shape from silicon powder and nitriding it at high temperatures. The volume changes very little in the nitriding process, and porosity range is usually 15-20%. Because it is free from sintering additives, nitrided silicon has much better creep properties than sintered nitride.

The methods to produce nitrides used in semiconductor processing are either a variant of the nitriding process above or through PECVD (plasma-enhanced chemical vapor deposition). Nitriding involves the high temperature nitridation of the silicon surface. PECVD nitride is created through the low temperature reaction of silane and ammonia in the presence of an RF field. Some select properties of high and low temp nitrides are given in Table 8.2.

Table 8.2: Select Properties of Silicon Nitride[37]

Property	**High Temp Nitride**	**PECVD**
Density (g/cm^3)	2.8-3.1	2.4-4.8
Hardness		
Knoop	1000-3500	–
Moh	9	–
Stress (10^9 dyne/cm^2)	12-18	-2 to +5
Coefficient of thermal expansion (10^{-6}/C)	4	4-7
Refractive index	2.08	2.0-2.2

Sintered monolithic silicon nitride (i.e., solid nitride without toughening reinforcements) has fracture toughness in the range of 4-6 MPa-$m^{1/2}$. This is slightly higher than most monolithic ceramics, but it is attributed to the tendency for β grains to grow in an elongated morphology. Toughness can be increased through appropriate strengthening mechanisms (e.g., fiber reinforcements), though they are not suitable for semiconductor manufacturing.

8.2.3 Silicon Carbide[38]

Silicon carbide is probably the most widely used non-oxide ceramic. Some of the properties that make it useful are high hardness, moderate strength, and good strength retention to high temperatures. Carbide exists in cubic form, termed beta form, and a variety of hexagonal and rhombohedral modifications collectively termed the alpha form.[39]

Pure silicon carbide powder does not sinter without pressure. Commercial carbide is made by one of four processes: second-phase bonding, reaction bonding, sintering, and the Acheson process. The form of silicon carbide used in semiconductor manufacturing is produced by the PECVD reaction of silane and a suitable hydrocarbon. Second-phase bonding involves using a mixture of SiC powder with resin, glass, silicon

nitride, clay, metal, or other material. Reaction bonded carbide is made by mixing SiC powder with carbon or silicon metal powder. In reaction-bonded material, carbon can react with the carbide vapor to forma silicon carbide bond or silicon can react with a nitrogen atmosphere to form a silicon nitride bond. The Acheson process involves mixing silica and coke in a large mound and placing large carbon electrodes in opposite ends. A current is passed between the electrodes and through the mound, which heats the coke to 2200^{o}C due to resistance heating. The coke reacts with the silica to form silicon carbide and carbon monoxide gas.

Daroudi, Tressler, and Kaprzyk measured the strength of siliconized silicon carbide tubes using a C-ring technique to measure the strength of the outer surface.[40] Short time strength was found to be about 50 MPa in tension up to 1350^{o}C. The stress-strain relationship is nearly linear up to 1000^{o}C, above which plastic deformation is evident.

8.3 Testing of Silicon, Ceramics, and Coatings

In testing these materials, one may look to the literature for guidance. We find that silicon may be tested a number of ways. Fischer et. al. tested silicon in a very traditional sense, and looked for the stress-strain relationship at high temperature.[12] Others have used micro-hardness indentation tests for bulk silicon.[41,42] More complex techniques have also been used; the K_{Ic} for <110> silicon has been reported using plasma etch technology to create MEMS.[43] In other literature, Bawa et. al. used still another method, ASTM standard test F394-78, for testing the proposed thickness of 300mm

diameter silicon wafers; they reported an MOR of 130 MPa for <100> silicon.[19] Clearly there is no standard procedure to characterize silicon, and discretion is left to the scientist to determine the best test rig for his material.

Following the literature further, one may discover a more uniform case for testing ceramic-coated materials. Andritschky et. al. used the un-notched four-point bending technique to measure the mechanical properties of a zirconia film on a steel substrate.[44] In a variation of three-point bending tension tests, Yoshioka et. al. used MEMS technology for testing 0.1μm SiO_2 and Si_3N_4 films on silicon die.[45] Yoshioka reported fracture strains of 2.5% and 3.8% for oxide and nitride, respectively.

There appears to be better agreement in the literature on the technique for testing coatings; three-point and four-point bending tests are among the better test methods. Using this as a guide, and considering the theory on tensile tests, four-point bending tests of ceramic coatings on silicon substrates appear to be a very valid approach to investigate the mechanical properties of a layered system.

8.4 Thin Film Experimental Method

8.4.1 Thin Film Deposition

To test the effect of a thin ceramic coating on the mechanical properties of silicon wafers, three CVD films (silicon nitride, silicon oxide, and silicon carbide) were coated on the front-sides of multiple different wafers. All three types of coatings were nominally 10,000Å thick. The oxide and nitride were deposited on 150mm diameter,

25mil thick wafers using an Applied Materials ® P5000 CVD tool and commonly available process recipes.

Silicon Nitride Deposition: $SiH_4 + NH_3 \rightarrow Si_3N_4 + 12H_2$

Silicon Oxide Deposition: $SiH_4 + N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$

The carbide was deposited using a method proprietary to Texas Instruments, Inc. Each film was deposited at a temperature of 400^{o}C. The wafers in each test group were all from the same supplier and ingot. The thickness of each film was measured by stereoscopic interferometry on a Prometrix FT-750. Select films were also measured on a Hitachi S-4700 scanning electron microscope, and the actual coating thickness ranged between 0.85 and 0.95μm (8,500 and 9,500Å). SEM images appear below in Figure 8.1.

By adjusting process parameters we were able to modify residual stress for each ceramic film. The parameters that were adjusted appear below in Table 8.3.

Table 8.3: Adjusted Parameters of obtaining films of various stress

Nitride	**Oxide**	**Carbide**
High Freq. Power	High Freq Power	Low Freq. Power
	Silane Flow	High Freq. Power

For each ceramic material, three films were created: “high,” “medium,” and “low” stress films. In the frame of this discussion, “high” stress means more compressive and “low” stress means less compressive or even tensile.

8.4.2 Thin Film Mechanical Characterization

a) Modulus of Rupture

After deposition, coated and uncoated wafers were cleaved into samples using a diamond tipped scribe and Fletcher “Gold Tip” ® glass nipping and breaking pliers. The size of each sample size was nominally 11mm x 10mm.

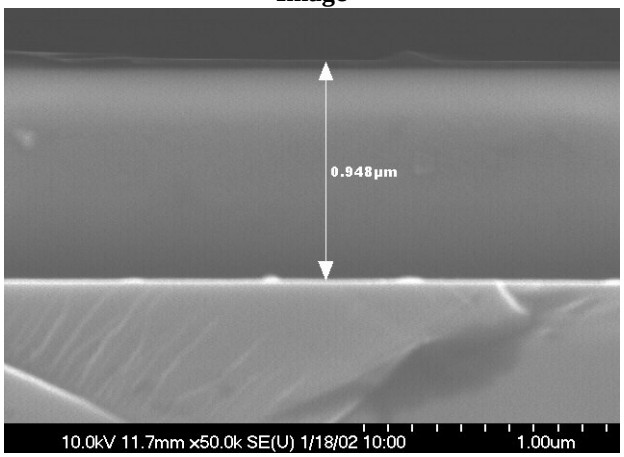
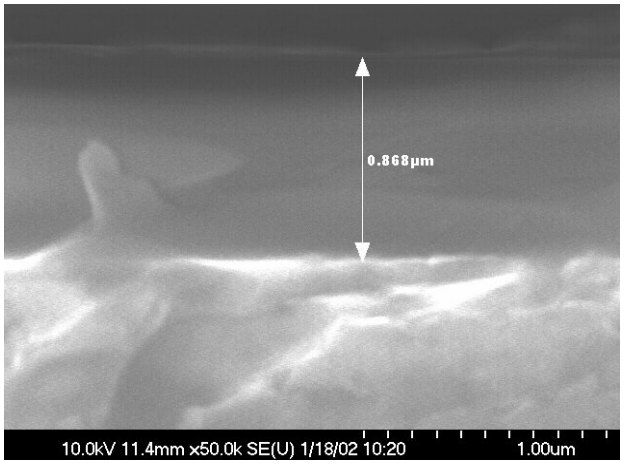
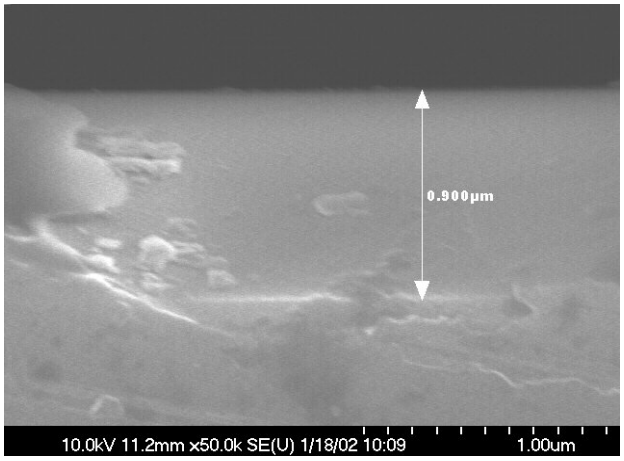
Coating	Image	Thickness (μm)
SiN 2		0.948
SiO 2		0.868μm
SiC 2		0.900μm

Figure 8.1: SEM images of the coated samples

The samples were tested both coating side up and coating side down. The coated silicon samples were tested against the baseline, uncoated silicon samples. An un-notched four-point bending test rig was used to test the samples.

The four-point bending test rig was selected over other methods that are commonly used (e.g., three-point bending and compact tension/fracture). Crystalline silicon is a brittle material, and the four-point method allows the force to be spread across a larger area of the sample. This increases the likelihood of containing a critical flaw in the stressed region. Also, owing to a less complex sample scheme, fabrication of a four-point bending sample is much easier than sample creation for the CT/FT test. Finally, the samples were left un-notched because the sample preparation process creates inherent defects (i.e., edge chips, microcracks, etc. during sawing).

An IMADA motorized test stand (MV-100) in conjunction with a digital force meter (DPS-110R) was used to measure the peak force to fracture each. The motorized stand was set at 0.40 mm/min. Figure 8.2 shows a schematic representation of the sample test rig. The force to fracture the sample in kg_f was recorded after each run. Twenty samples of each type of coating were run in order to compare test data between groups.

b) Residual Stress

The residual film stress of each coating was measured using a stress measurement system.

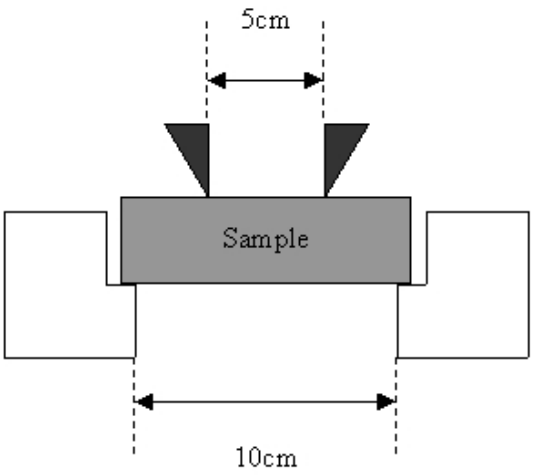


Figure 8.2: Schematic Representation of the 4-Point Bend Test

The instrument determines the bow in the wafer before and after film deposition using Stoney's equation (Equation 8.1):[46]

$$\sigma_r = \frac{E t_s^{\,2}}{6(1-\nu)t}\left(\frac{1}{R_f} - \frac{1}{R_o}\right) \tag{8.1}$$

where E is the Young's modulus of the substrate, ν is Poisson's ratio of the substrate, t_s is the thickness of the substrate, t is the thickness of the film, and R_o and R_f are the initial and final radii of curvature, respectively, of the wafer before and after film growth.

c) Adhesion Strength

The effect of thin film adhesion on mechanical properties was investigated. Good layer adhesion will be necessary for the coating to survive the fab-processing environment. Scaling or flaking of the coating will be unacceptable since the flaking particles could adversely affect electrical yield. Thin film adhesion was characterized by 4-point bending using a technique developed by Dauskardt.[47, 48]

In Dauskardt's method, samples of appropriate size are created from the coated wafers. In this work, the nominal sample dimensions were 50mm x 10mm. Once the

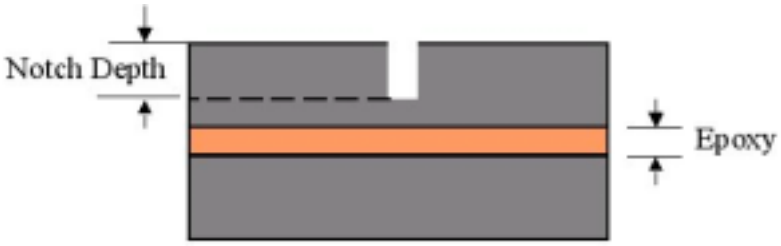
samples are cleaved to size, a thin layer of epoxy (~3mil of Allied High Tech Epoxy Bond 110) is sandwiched between two samples with the ceramic-coated sides facing each other. Figure 8.3 depicts the sample configuration. This configuration is chosen so that the maximum shear stress is applied on the sample (see section 4.3.4).

Figure 8.3: Adhesion Strength Sample Geometry

Once the sample was created, a diamond saw was used to create a pre-notch. The saw was a Disco model DAD-2H/6, and the dicing wheel was a Semite model F1225. The pre-notch is cut to within a few microns of the first interface. Figure 8.4 provides a representative and an actual image of pre-notched samples.

A high-stiffness micromechanical test system using a piezoelectric actuator was used to load the samples under displacement control with ramp rate varying between 0.5 and 8.5 μm/sec. The load was applied to the side of the sample that was opposite the pre-notch; loads were measured and recorded as a function of the loading pin displacement.

a)



b)

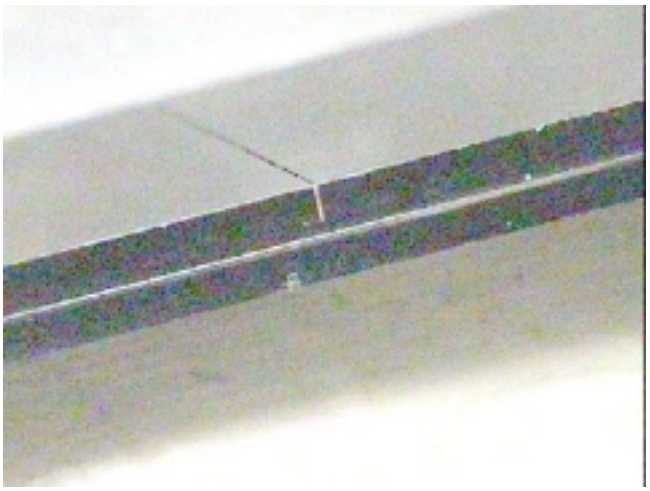


Figure 8.4: Pre-notched sample a) representative image, b) actual sample image taken at an angle, notch side facing up

The driving force for debonding/delamination can be expressed in terms of strain energy release rate *G* if plasticity near the debond tip is limited. Using beam theory, *G* is given as[49]:

$$G = \frac{21(1-\upsilon^2)M^2}{4Eb^2h^3} \tag{8.2}$$

where *E* and ν are the elastic modulus and Poission's ratio of the bulk substrate, respectively; the bending moment *M* equals *PL/2*, with *P* being the load and *L* the spacing between the inner and outer lines; *b* is the sample width; and *h* is the half thickness. If the quantity $(1-\nu^2)$ is assumed to be approximately unity, the above equation becomes:

$$G = \frac{21M^2}{4Eb^2h^3} \tag{8.3}$$

For silicon, ν is about 0.28, so (1-ν^2) is about 0.92. Since 4-point bending measures mixed mode adhesion strength, the phase angle of loading (ratio of shear to normal stress) is typically 43 degrees.[47,50,51] For 4-point bending, *G* is independent of debond length when the debond is more than two times the total beam thickness.

A typical load-displacement curve for a delaminating sample appears below in Figure 8.5. This can be characterized as an adhesion failure, where the film delaminates from the substrate.

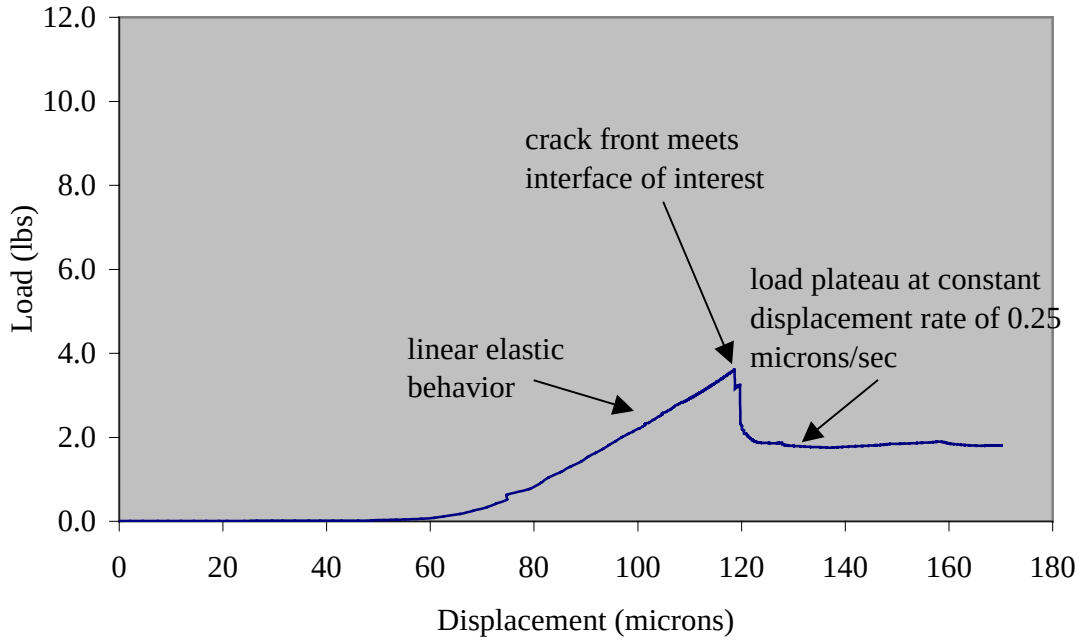


Figure 8.5: A typical load-displacement curve for debonding along Si/thin film interface. Features of the curve corresponding to cracking events are indicated.

Here the crack propagates through the silicon and then laterally at the interface of the film/substrate.

In a cohesive failure, the film does not delaminate from the substrate. Rather, the pre-crack continues to the interface of the sample where the elastic behavior of the substrate continues to dominate. The load on the sample increases until either the epoxy or sample fails without film delamination. Thus, the failure is cohesive. In this scenario, the film-substrate bond is at least as strong as the Si-Si bond in the substrate. Figure 8.6 shows a load displacement curve for a cohesive sample failure.

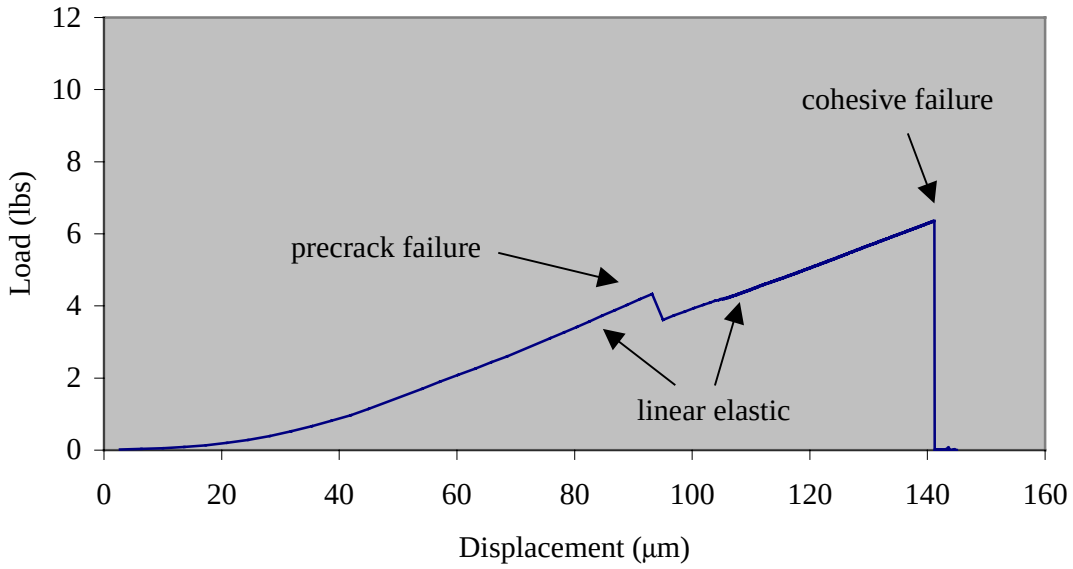


Figure 8.6: A typical load-displacement curve for cohesive failure. Features of the curve corresponding to cracking events are indicated.

d) Modulus and Hardness

The bulk mechanical properties of the base films (i.e., SiN 2, SiO 2, and SiC 2) were evaluated by nanoindentation to determine the modulus *E* and hardness *H*. (See Tables 8.4 and 8.8 for further clarification of film properties.) The tests were performed on an MTS Nano Indenter ® SA2 using continuous stiffness measurements (CSM) and a low load head (DCM) and a 50nm Berkovich tip.

The measured stiffness from the load versus displacement data are converted to the modulus by the following formula[51]:

$$E_r = \frac{\sqrt{\pi}}{2}\frac{S}{\sqrt{A}} \tag{8.5}$$

where E_r is the reduced modulus, S is the measured stiffness, and A is the contact area between the indenter tip and the material. Young's modulus, Poisson's ratio, and the coefficient of thermal expansion (CTE) are the material parameters required for the stress analysis

Hardness is the trend to permanent deformation, and it is determined by[51]

$$H = \frac{P_{\max}}{A} \tag{8.6}$$

where P_{max} is the peak load and A is the projected area of the indenter at the peak load and varies with the indenter geometry (see section 4.3.3). Smaller indentations at fixed loads mean less contact area and harder materials.

8.4.3 Thin Film Chemical Characterization

The thin film materials were characterized by Rutherford backscattering spectroscope (RBS) and fourier-transform infrared spectroscopy (FT-IR) techniques. RBS was used to determine composition, and FT-IR was used to determine bonding strength of each film.

The elemental composition of each film was determined by RBS. The RBS measurements were done using a 2.275 MeV He^{2+} ion beam on a van de Graff accelerator from a commercial vendor.

A Thermco Nicolet ECO-8M infrared spectrometer was used to determine chemical bonding strength for each film. The spectral resolution was set at $4cm^{-1}$, and the center of each wafer was scanned over 100 times to obtain a spectrum. The FT-IR scan range was between $4000cm^{-1}$ and $400cm^{-1}$. The layer absorbance of the film was determined by subtracting the absorbance of the respective uncoated wafer.

8.5 Ceramic Thin Film Test Results and Discussion

8.5.1 Thin Film Chemistry

The Si/X ratio, where X = C, O, or N, of the deposited films was determined by the RBS technique. The results are given in Table 8.4.

Table 8.4: Thin Film RBS Data

Sample	Residual Film Stress (MPa)	Si/X ratio
SiN 1	238.3	1.695
SiN 2	-141.9	0.962
SiN 3	-489.1	0.855
SiO 1	10.4	0.588
SiO 2	-130.9	0.538
SiO 3	-225.2	0.515
SiC 1	-332.3	0.972
SiC 2	-476.3	1.074
SiC 3	-529.9	1.193

For the silicon nitride samples, the effect of the variation in power can be seen in the composition ratio. Decreasing power moved the film further away from stoichiometric ratios while moving the film stress from compressive to tensile. RBS indicates a constant Si/N ratio for all films through the entire film.

For silicon oxide, increasing the silane flow and reducing the power affected the film by increasing the silicon content in the film. It also moved the composition further away from stoichiometric ratios, though not as drastically as with the silicon nitride. As with the nitride films, the Si/O ratio was constant throughout the depth of the oxide films.

In the carbide RBS data we find that changing the power results in stoichiometric shifts in the film. Raising the low frequency power and reducing the high frequency power resulted in higher residual stress values and makes the films more silicon-rich. RBS also indicates changes in the Si/C ratio through the depth of the film, though the cause for the change in ratio with depth is unknown. The data presented in Table 8.4 represent an average of the Si/C ratio through the depth of each film.

8.5.2 Molecular bonding

The IR spectra of the SiN films with different film stresses can be seen in Figure 8.7.

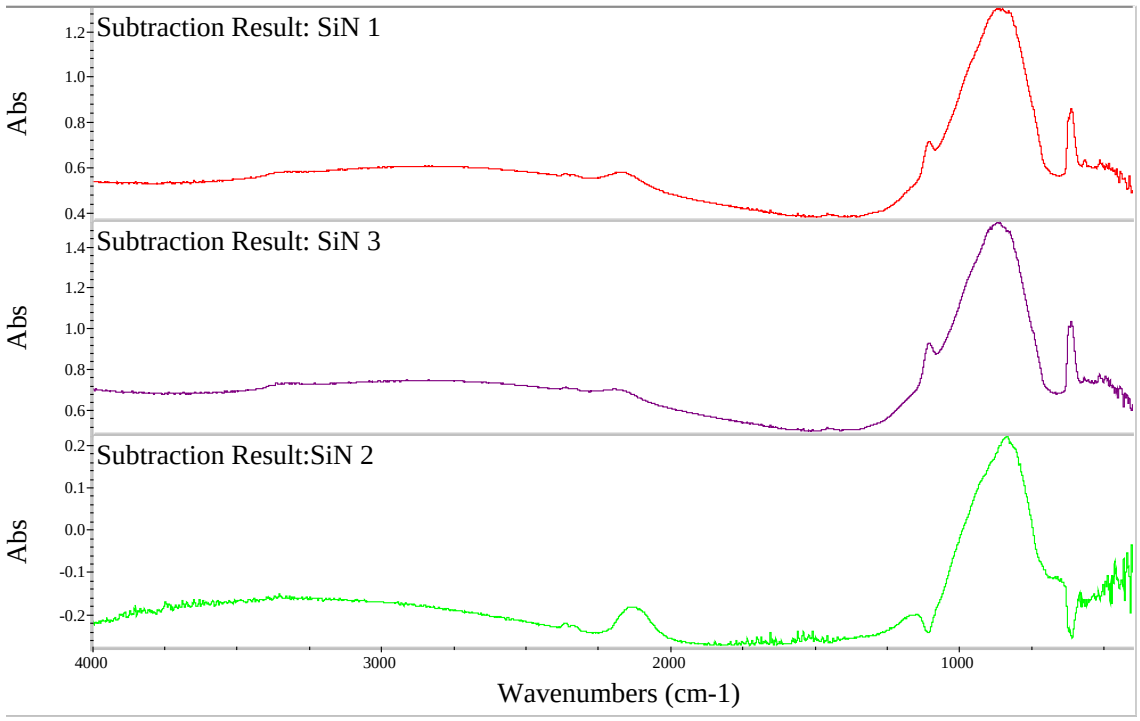


Figure 8.7: SiN FT-IR Results

The PECVD films show a strong Si-N absorption peak (830-850 cm^{-1}) and weak peaks of Si-H (~2160 cm^{-1}). The main Si-N absorption peak is shifted to lower wavenumbers in the SiN 2 film; this shift is about 40cm^{-1}. The tensile film, SiN 1, and high-compressive film, SiN 3, show some small evidence of N-H absorption (~3340 cm^{-1} and ~1060 cm^{-1} shoulder peak). The main N-H peak is indistinguishable from the background of the high-compressive stress SiN 2 film; a small shoulder peak does exist, although slightly shifted. The same two films show evidence of stronger Si-Si bonding (~610 cm^{-1}).

The IR spectra of the SiO films with different film stresses can be seen in Figure 8.8.

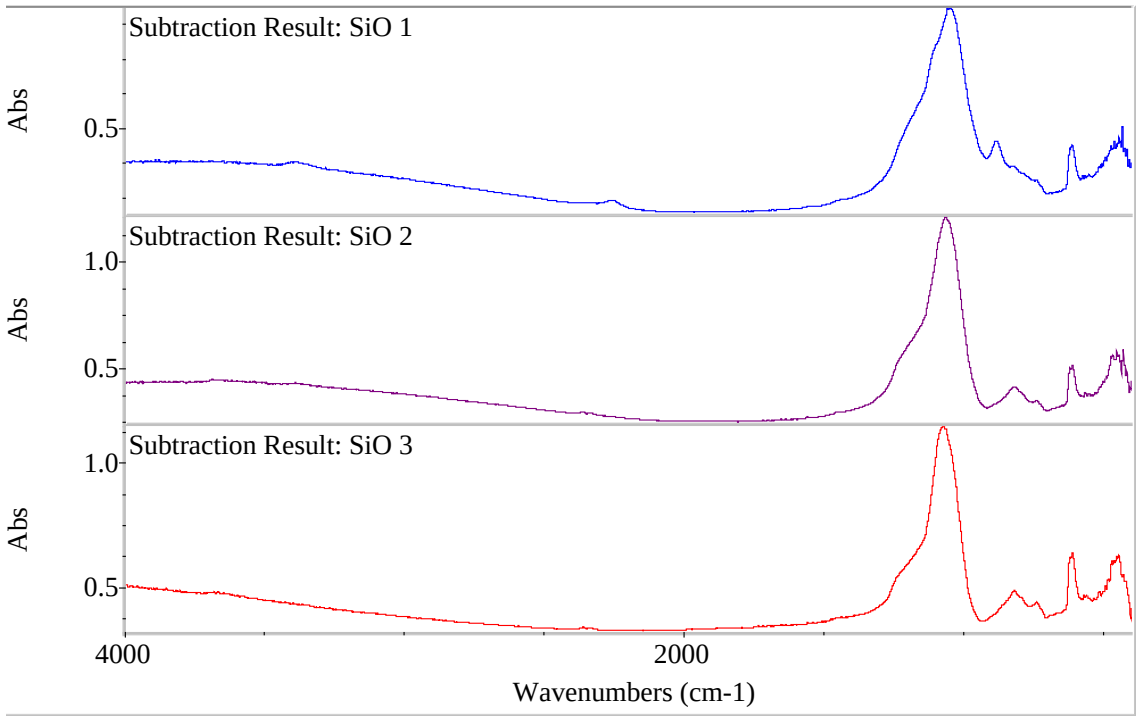


Figure 8.8: SiO FT-IR Results

The oxide PECVD films showed strong Si-O absorption peaks (1050-1070 cm^{-1} and ~820 cm^{-1}) and weaker Si-Si absorptions (~610 cm^{-1}). The Si-O absorption peak shifts to higher wavenumbers as stress increases (~20 cm^{-1}), signifying changes in bond strength as a function of stress. The tensile film, SiO 1, showed a small Si-H absorption peak (~2230 cm^{-1}) that was not exhibited in the other two oxide films. Small N-H shoulder peaks (~1250 cm^{-1}) exist for all the oxide film.

The IR spectra of the SiC films with different film stresses can be seen in Figure 8.9.

Figure 8.9: SiC FT-IR Results

All carbide PECVD films showed strong Si-C absorptions (~800 cm^{-1}). The SiC absorption peak shifts to higher wavenumbers as residual stress increases; this shift is about 10cm^{-1}. SiO_2 impurities may be responsible for the band at 1000 cm^{-1}. In each film, clearly observable Si-H absorptions can be seen at ~2090 cm^{-1}. Bonds of C-H are evident by small peaks at ~2900cm^{-1}. Finally, all films showed Si-Si absorption at ~610 cm^{-1}, though the peak is less pronounced in the high-compressive stress silicon carbide film. FT-IR suggests that there is not much difference in the bond strength of the three different carbide films since all three spectra look very similar, though RBS showed differences in stoichiometry.

8.5.3 Thin Film Mechanical Characterization

a) Modulus of Rupture

The four-point bending test results of the coated and uncoated samples appear below in Figure 8.10. The data presented in Figure 8.10 are for the tests with the coated side up only. The standard deviation for the data with the coated side down was almost 100% of the average. For each of the tested sample types, the MOR (Equation 4.13) was calculated. From the figure, we see that bare silicon had an average MOR of 139.69 MPa, SiN-coated samples had an average MOR of 125.7, 144.9, and 145.2 MPa, respectively; SiO-coated samples had an average MOR of 134.0, 142.4, and 146.8 MPa, respectively; and SiC-coated samples had an average MOR of 153.4, 159.2, and 164.0 MPa, respectively. The standard deviation for each group will be reported as a percentage of the average value MOR (i.e., standard deviation divided by the average). The values are 18.2% for the silicon samples; 20.7%, 16.6%, and 21.1%, respectively, for the SiN samples; 17.2%, 21.4% and 15.3%, respectively, for the SiO samples; and 20.7%, 22.9% and 17.8%, respectively for the SiC samples.

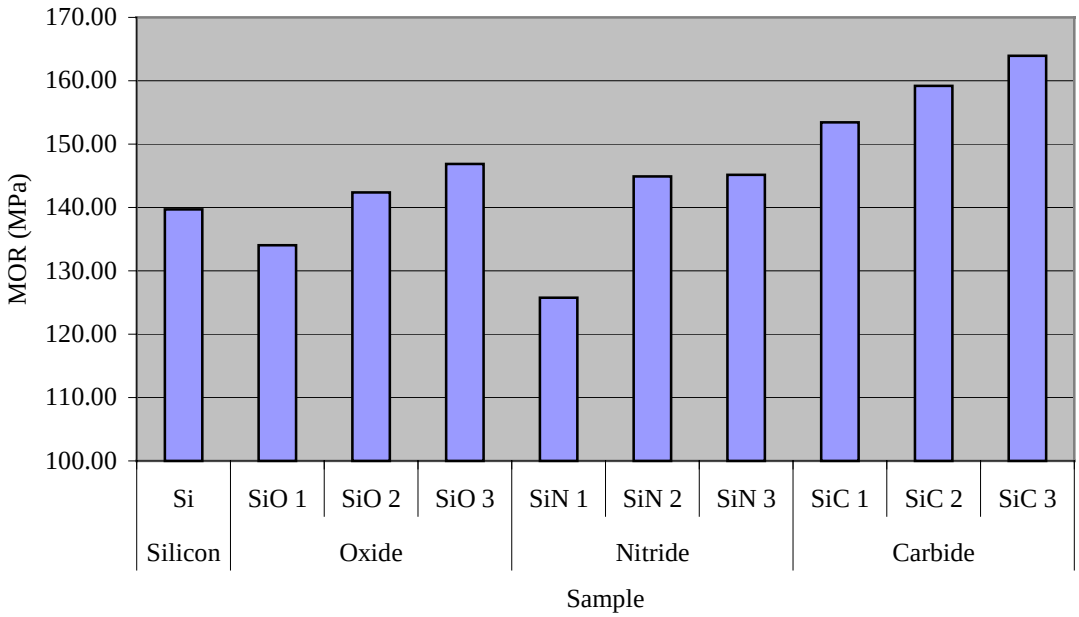


Figure 8.10: Average MOR values by sample type

Data for the samples tested with the coating side away from the load will not be presented because the standard deviations for those tests were nearly 60 to 100% of the average. The wide spread in the data is attributed to the finely polished surface of the silicon substrate. The backside of the wafer is much "rougher" in comparison to the front. The roughness presents flaws for cracks to begin propagating, and the backside is likely to contain such a flaws. The front-side of the wafer is designed to be as close to flawless as possible. Without a flaw for crack initiation, a sample tested in such a manner will show relative strength. (This is also the reason why bending beam samples are often notched.) However, if a micro-flaw exists, the potential for crack initiation increases drastically due to stress concentration.

Figure 8.11 compares the coated samples by calculating the gain in the MOR over the uncoated samples. Here we see that, depending on the sample, SiN coatings offer a

change from -10% to roughly 4% in the MOR; SiO coatings over a change from -4% to roughly 5% over uncoated silicon; and the SiC samples showed a change of about 10% to 17% in mechanical properties.

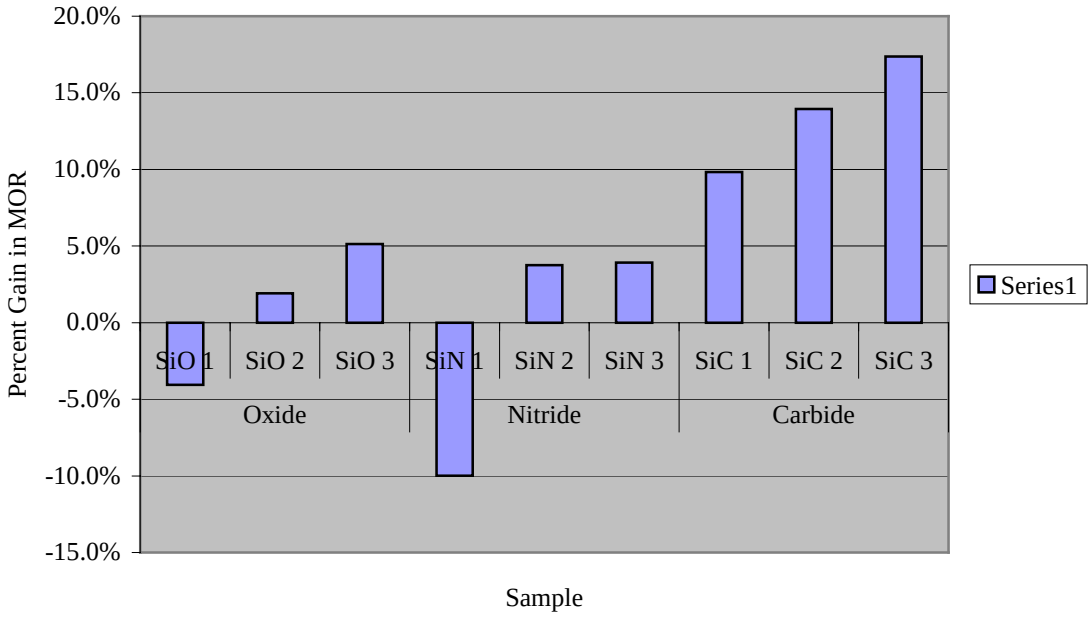


Figure 8.11: Coating strength gain as a percentage of the uncoated sample

Using Equation 4.13, the modulus of rupture was calculated for each sample using the four-point bending geometry given in Figure 4.5b. *P* was the experimentally determined maximum force (given in kg_f). The value *a* was fixed at 2.5 mm, *d* was fixed at 625 μm, and *b* was 10 mm. For uncoated <100> silicon, the calculated MOR value was 139.7 MPa.

Table 8.5 shows the average MOR in MPa data by sample, average overall data (x-bar) by sample type, the standard deviation (σ) by sample type, and the standard deviation divided by the average by sample type.

Table 8.5: Aver MOR (MPa) by sample type

	Nitrides			Oxides			Carbides		
	SiN 1	**SiN 2**	**SiN 3**	**SiO 1**	**SiO 2**	**SiO 3**	**SiC 1**	**SiC 2**	**SiC3**
Ave MOR	*125.7*	*144.9*	*145.2*	*134.0*	*142.4*	*146.8*	*153.4*	*159.2*	*164.0*
σ	21.58	31.02	22.26	27.7	23.6	31.0	31.8	36.4	29.2
σ over MOR	*20.7*	*16.6*	*21.1*	*17.2*	*21.4*	*15.3*	*20.7*	*22.9*	*17.8*

Bawa et. al. found a MOR value of 130 MPa for 300mm silicon wafers, however the technique employed in those experiments was ASTM standard F394-78.[19] As already discussed, sample size and test technique will affect the apparent material strength measurement if the flaw size has an appreciable distribution. Since sample sizes are very different, it is only appropriate to compare the sample size data relative to one another. The data reported here are for much smaller samples and are for four-point bending tests. Based on the discussion in *Section 4.3.4*, it is fair to expect the data to show some relative strength compared to the MOR reported by Bawa.

Richerson provides some MOR data by ceramic type.[52] Some of these select MOR values appear in Table 8.6. If it were possible to generalize the data in the table, we would expect to find that carbide and nitride should compare better than an oxide with all other things being equal. This was not the case, however, in this set of experiments.

Table 8.6: Select ceramic MOR values at room temperature

Material	**MOR (MPa)**
Si_3N_4 (Hot-pressed , <1% porosity)	620-965
Si_3N_4 (Sintered, ~5% porosity)	414-850
Si_3N_4 (Reaction bonded, 15-25% porosity)	200-350
SiC (Hot-pressed, <1% porosity)	621-825
SiC (Sintered, ~2% porosity)	450-520
SiC (Reaction-sintered, 10-15% free Si)	240-450
SiC (Bonded, ~20% porosity)	14
SiO_2 (fused)	110

Several theories exist that might explain the difference in comparison of the experimental data to literature data. According to Andritschky, [44] the effects of residual film stress on a system may be significant. This will be discussed further.

b) Residual Stress

As mentioned above, residual film stress can play a significant factor in determining the mechanical performance of a film. Film stress σ_f is comprised of three principle constituent elements as shown in Equation 8.7:

$$\sigma_f = \sigma_{th} + \sigma_i + \sigma_e \tag{8.7}$$

where σ_{th} is the thermal contribution due to mismatches in the CTE; σ_i is the intrinsic stress and is related to microstructure (i.e., morphology, grain size, texture, etc); and σ_e is the extrinsic stress which deals with the adsorption of molecules that may penetrate into pores of undensified films.[53, 54] If one assumes that the film is fully densified or that no molecules have been adsorbed, Equation 8.8 is simplified:

$$\sigma_f = \sigma_{th} + \sigma_i \tag{8.8}$$

Equation 8.7 reduces the residual stress equation to factor thermal and intrinsic contributions. This appears to be an acceptable approach for semiconductor thin films.[55]

Thermal film stress can be calculated from the following equation[50]:

$$\sigma_{th} = \frac{(\alpha_f + \alpha_s)E_f \Delta T}{1 - \nu_f} \tag{8.9}$$

where α_f is the CTE for the film, α_s is the CTE for the substrate, E_f is Young's modulus of the film, ΔT is the change in temperature for the film at the time between film deposition and film stress measurement; ν_f is Poisson's ratio for the film.

The residual stress was measured using a stress measurement system. Table 8.7 summarizes the measured residual stress and other thermal and mechanical properties of the ceramic coatings.

Table 8.7: Select thermal and mechanical properties of silicon and silicon-based ceramics

Material Property	**Si**	**SiN**	**SiO**	**SiC**
a (K^{-1})	2.30E-06 [56]	3.60E-06 [57]	5.00E-07 [56]	4.30E-06 [58]
E_f (dyne/cm^2)	n/a	3.03E+12 [59]	7.00E+11 [59]	4.17E+12 [59]
ν_f	n/a	0.24 [59]	0.17 [56]	0.14 [59]

Table 8.8 summarizes the measured thin film stresses and the standard deviation in each group. Implicit in the calculated values is that the CTE for the base material is the same for all films within the test group. That is, for example, CTE(SiN) = CTE(SiN *i*).

Table 8.8: Residual Thin Film Stress Statistical Data

Film	**Ave. Measured Film Stress (dyne/cm^2)**	**Std. Dev.**	**Calculated σ_{th} (dyne/cm^2)**	**Calculated σ_i (dyne/cm^2)**
SiN 1	2.38e9	2.08e6	1.94e9	4.36e8
SiN 2	-1.42e9	5.77e5	1.94e9	-3.36e9
SiN 3	-4.89e9	1.07e7	1.94e9	-6.84e9
SiO 1	1.04e8	1.01e6	-5.69e8	6.73e8
SiO 2	-1.31e9	1.33e7	-5.69e8	-7.41e8
SiO 3	-2.25e9	5.77e5	-5.69e8	-1.68e9
SiC 1	-3.32e9	1.53e6	3.64e9	-6.96e9
SiC 2	-4.76e9	5.77e5	3.64e9	-8.40e9
SiC 3	-5.30e9	3.46e6	3.64e9	-8.94e9

Figure 8.12 shows a graph of MOR as a function of film stress with a linear regression fit. For the linear fit, R-squared equals 0.825, and the y-intercept is 136.5 MPa. This means that at zero residual stress, the mechanical properties of the film-substrate system should equal 136.5 MPa. Since the thickness of the film is much smaller than the thickness of the substrate ($t_f << t_s$), we expect that the mechanical properties of the substrate dominate. If this is true, the y-intercept and the MOR of uncoated silicon

should be within experimental error of each other. There is only a 2.3% difference between the MOR of silicon and the expected MOR of a coated sample with no film stress.

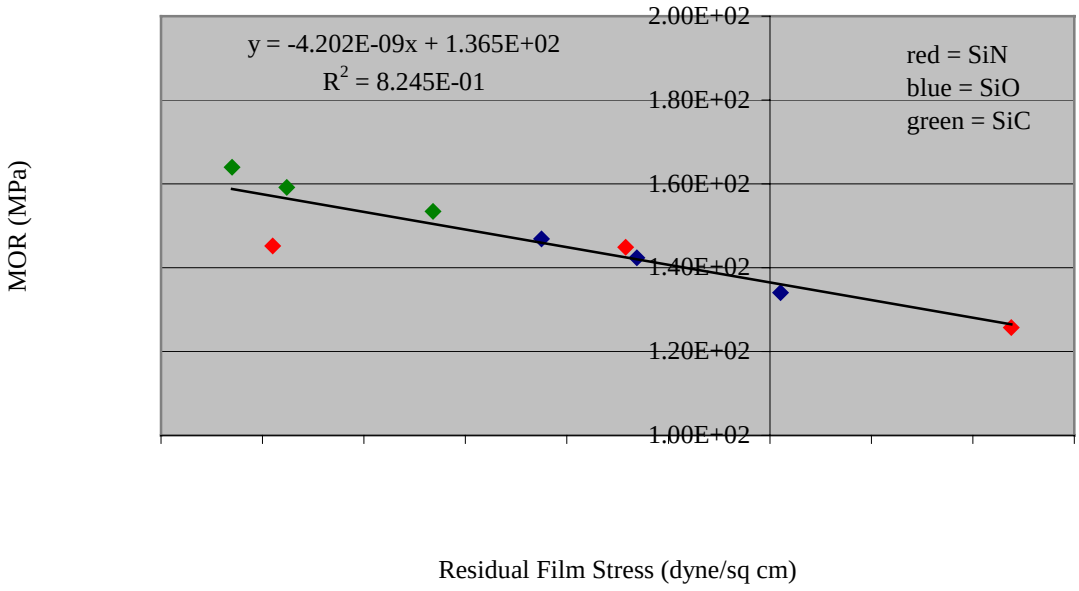


Figure 8.12: MOR as a function of film stress

Furthermore, we see that there is one point along the trendline that does not fit near as well as the others. This point corresponds to the SiN 3 film, or the one that experienced adhesive failure during testing. As mentioned earlier, every other film exhibited cohesive failure. If this point is removed from the graph for the sake of "apples-to-apples" comparison (i.e., including only the films where cohesion was the fail mode), the R-squared value becomes 0.990; clearly, this is a much better fit for the data.

Thus, for a coated sample, the determining factor of the coatings mechanical usefulness will be its residual stress. It seems that this must be considered in conjunction with the films adhesion strength. For a material in tension, the applied force must

overcome the residual stress of the coating. At this point the coating fails, and the mechanical properties of the substrate dominate. Using this concept to interpret the data above, we find that the coated material response is entirely reasonable. Andritschky et. al. have also arrived at a similar conclusion in analyzing zirconia-coated steel substrates.[44]

To summarize the results, modulus of rupture for a ceramic-coated silicon sample appears to be related to the residual stress in the film. MOR increases with increasing compressive stress, but also appears dependent upon thin film adhesion.

c) Adhesion Strength

Between seven and ten samples were tested for each different film. The results of the thin film adhesion test are given in Table 8.9. Only one film type exhibited adhesive failure; that was SiN 3, the high compressive stress nitride film. Every other film exhibited cohesive failure. If the film exhibited adhesive failure, the sample was optically inspected to determine the location of the failure at the interface. Adhesion fails were easily verified since one half of the failed sample had the ceramic film while the other did not. Cohesive failure was also verified by optically inspecting the sample. For the cohesive failures, however, the debond length was not greater than twice the thickness of the sample or there was not debonding whatsoever. In many cases, epoxy failure was evident due to scarring or peeling of the adhesive layer from the underlying film.

Table 8.9: Thin Film Adhesion

	Nitrides			Oxides			Carbides		
	SiN 1	**SiN 2**	**SiN 3**	**SiO 1**	**SiO 2**	**SiO 3**	**SiC 1**	**SiC 2**	**SiC3**
Film Stress (MPa)	*238.3*	*-141.9*	*-489.1*	*10.4*	*-130.9*	*-225.2*	*-332.3*	*-476.3*	*-529.9*
Type of Failure	cohesive	cohesive	adhesive	cohesive	cohesive	cohesive	cohesive	cohesive	cohesive
Location of failure	*Si*	*Si*	*Si/SiN*	*Si*	*Si*	*Si*	*Si*	*Si*	*Si*
Adhesion Strength (J/m^2)	N/A	N/A	1.49	N/A	N/A	N/A	N/A	N/A	N/A

d) Modulus and Hardness

The results of the nanoindentation tests are given below in Table 8.10. To calculate a single value for the bulk modulus and hardness of each film, the data were averaged at ~10% of the film thickness, where there is usually a plateau in the hardness/modulus data.

Table 8.10: Nanoindentation tests

Film	**Hardness (GPa)**	**Modulus (GPa)**
SiN 2	16.71	164.16
SiO 2	7.81	74.92
SiC 2	20.34	167.48

For a film that is ~1 μm thick, the plateau will usually be somewhere between 50-100 μm. This helps to avoid influences on the data from the underlying substrate. While not every film could be measured, the data for the base films are expected to fairly represent the other films (e.g., SiN 2 data is close to SiN 1 and SiN 3).

For each of the measured films, the modulus is less than the fully dense theoretical value. This can suggest one of two things: 1) either the film is not fully dense, or 2) the compositional effect shifted the mechanical properties from those of the stoichiometric materials.

8.6 Cost Analysis

Cost is one aspect to consider in using coated wafers for mechanical support. If an idea costs more to a company than it might potentially save, then there is little financial reason to pursue it. The following discussion is a simple cost analysis for using coatings as a means to improve yield, and thereby increase revenue.

In establishing a model for cost, one needs to determine what variables to consider and what to hold constant. In this analysis, there are a number of different variables: cost of the coated wafer, baseline process yield, and revenue per wafer are some of the factors. Table 8.7 provides some shows some of the factors to be considered. The factors under investigation in this analysis are starred (*).

Table 8.11: Baseline Conditions for Cost Analysis of Coated Wafer

Base Parameter	Variable	Value
Coated Wafer Cost*	*A*	$100
Wafer Starts/Month	*B*	10000
Process Yield	*C*	95%
Wafers Saved/Month due to coating*	*D*	0%
Revenue/Wafer	*E*	$1000

* Under investigation

To evaluate the effect of the cost of the coated wafer and the estimated wafers saved due to the coating and its enhancement of the wafers mechanical properties, the

following equation was used to calculate the effect on net revenue (substituting the appropriate variable):

$$\text{Net Revenue} = A * B * C * D * E \tag{8.10}$$

The analysis assumes that implementation of a pre-stressed coating on the backside of a wafer will result in a positive effect on process yield; thus, some additional percentage wafers will be completely processed instead of broken.

A sensitivity diagram is presented in Figure 8.13. In the creating the graph, either the coated wafer cost *A* or the wafers saved/month due to the coating *D* were varied +/– 15% of their base value to find out the potential effect to net revenue assuming all other variables remained constant. From the graph, we find that the cost of the coating has a larger affect on net revenue than does the revenue generated due to increased process yield.

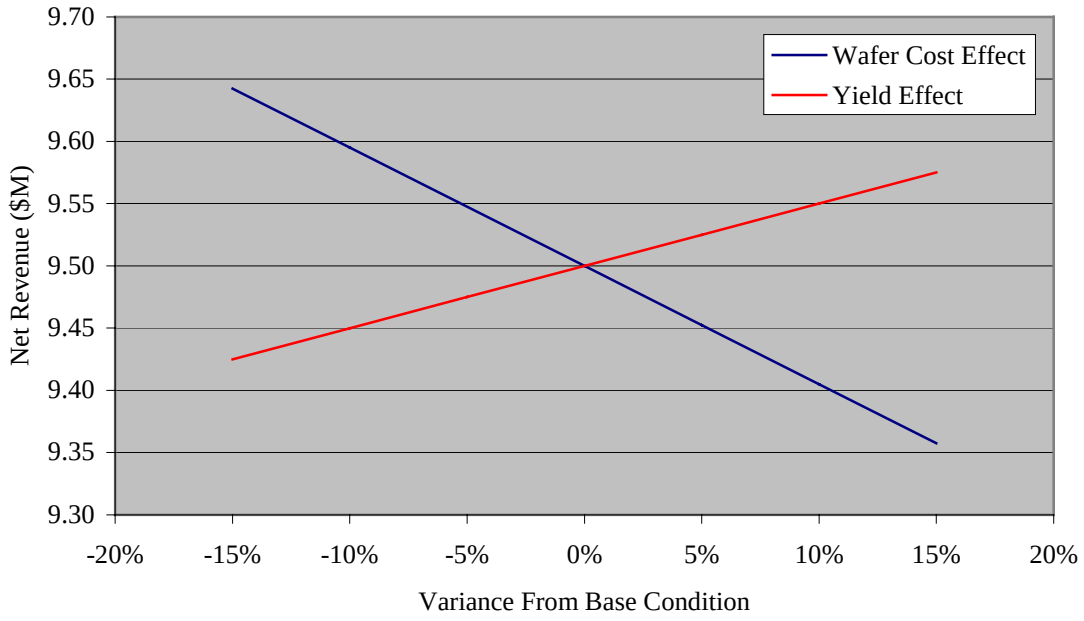


Figure 8.13: Net Revenue Sensitivity Diagram

This figure suggests that in order to maximize revenue on this project, the wafer should be obtained for the lowest possible cost. Likewise, one should seek to obtain the highest impact to yield. Both of these conclusions are intuitive.

In addition, it is estimated that the cost of the coating would add a few dollars to the cost the wafer. Assuming that the cost per wafer were to increase by five dollars and under the additional assumptions in Table 8.11, the coating would have to save just over 10% of the wafers per month that would normally be scrapped in order to be beneficial. Ten percent translates to saving 42 additional wafers per month. Of course, actual numbers and data should be used in place of those in Table 8.11 in order to determine the cost effect to a given factory.

8.7 Conclusions

As a result of this work, the following conclusions have been reached: 1) thin film coatings may be an acceptable means to increase the mechanical properties of silicon wafers, 2) residual stress is the primary factor in determining a film's usefulness for mechanical enhancement, and 3) the higher the residual stress in a thin film, the greater the effect on the mechanical properties.

CHAPTER 9: SUMMARY

9.1 Effects of the Barcode Dot Density and Chemical Etching on Wafer Strength

Three-point bending was used to evaluate the effect of barcode dot density on mechanical strength. The barcode is a stress concentration in the wafer. Wafers of two densities were tested; less dense barcodes were stronger than the wafers with higher densities. The wafer at the barcode is one-fourth to one-third as strong as the wafer in other areas. In addition, the data for the effect of chemical processing on silicon wafers indicate that isotropic etching is less likely to affect wafer strength than anisotropic etching. All other things being equal, isotropically etched wafers were twice as strong as anisotropically etched wafers.

9.2 Effects of Edge Bevel Design on Wafer Strength

Drop and strike tests were utilized to determine the effect of wafer edge bevel design on mechanical strength; five different profiles were tested. In general, a more rounded and uniform profile resulted in a stronger bevel. Round and smooth profiles follow classical structural designs, and distribute forces more uniformly. Brittle materials like silicon benefit from these profiles because external stresses result in internal compressive forces. Silicon is less likely to fail under compressive force than tensile force.

9.3 Effects of Structural Thin Films on Wafer Strength

Four-point bending was used to evaluate three different types of ceramic thin-film coated samples: silicon oxide, silicon nitride, and silicon carbide. The samples with the highest residual film stress, as determined with commercial measurement equipment, performed the best. This is because the applied force in the four-point bending must overcome the internal residual film stress prior to bulk silicon failure. Thin film coating chemistry is secondary to residual film stress in determining the effect to bulk mechanical properties.

CHAPTER 10: FUTURE WORK

10.1 Edge Bevel Design

The analysis of the edge bevel design and its affect on wafer breakage was only performed on 125 mm wafers in this work. There are, however, many different wafer diameters that are manufactured. The scope of future work would encompass optimum designs for each of these wafer diameters.

10.2 Barcode Dot Density

In light of the test data, a short-term project has been initiated with all wafer suppliers at the wafer fab facility. The project will see the reduction of the barcode dot density to 22 dots per line. Further reduction is not possible due to limitations in barcode technology. When scanned over a surface, a barcode reader looks for contrast differences in reflected light to read data. Decreasing the density might increase wafer strength, but it could also render the barcode unreadable. A longer-term solution is required.

An alternative approach to identifying wafers in the production facility is being investigated as a result of this work. This method would involve Optical Character Readable (OCR) technology. Instead of a barcode, human (and machine) readable alphanumeric characters are scribed on a wafer. While the OCR characters themselves may still represent stress concentrations on the wafer, the variability in the scribe position to create a character versus a straight line is expected to diminish the effect on wafer strength. The estimated payback for this method is about one year.

10.3 Coatings for Mechanical Characteristics

As previously mentioned, there are a few potential areas that future work might explore. First, the initial tests were performed on the front of a polished wafer. If this idea were to see light in a fab manufacturing environment, the coating would need to be on the backside of the wafer, possibly on double-sided polished wafers.

In addition, these coatings were deposited using PECVD processing. While acceptable for the initial tests, thermal coatings are generally much cleaner processes. A cleaner process will generally ensure that device physics are not disturbed since the threat of contamination is greatly reduced (i.e., no mobile metallic ions). Because of the proliferation of silicon oxides and carbides in use as fixtures for thermal operations (e.g., boats), it is not expected that these materials will affect devices physics. Furthermore, silicon oxide and nitride are already in use as thermally deposited and/or grown materials. In fact, oxide and polysilicon coatings are sometimes used as backside coatings for the purpose of defect gettering. Their use has been well characterized already. However, as a precaution, future tests should verify that thermal coatings on the backside of wafers would not affect reliability or device physics.

Finally, one should also explore how the thermal processing of a coated wafer affects the potential for wafer bow/warp during thermal operations. Residual stress exerted on a wafer by a backside film might cause the wafer to warp if not properly balanced or if it were to exceed the mechanical capability of the wafer. Several factors will potentially influence the maximum allowable film stress. To name a few, maximum

film stress is likely to be dependent upon the thickness of the wafer, processing equipment capabilities (such as photolithography equipment), and thermal processing conditions. These are some of the things to consider when evaluating the effects of film stress on wafer flatness.

APPENDIX: EQUIPMENT LIST

1. Applied Materials, Inc., 3050 Bowers Ave., Santa Clara, CA 95054, USA, http://www.appliedmaterials.com/.

2. Disco Hi-Tec America, Inc., 3270 Scott Blvd. Santa Clara, CA 95054, USA, http://www.discousa.com/.

3. Hitachi High Technologies America, 3100 N. First St., San Jose, CA 95134, USA, http://www.hitachi-hii.com/.

4. Imada, Inc., 450 Skokie Blvd., Suite 503, Northbrook, IL 60062 USA, http://www.imada.com/.

5. MTS Systems Corporation, 14000 Technology Dr., Eden Prairie, MN 55344, USA, http://www.mts.com/.

6. Prometrix (owned by Therma-Wave), 4221 Freidrich Lane, Suite #170 Austin, TX 78744, USA, http://www.therma-wave.com/.

7. The Fletcher-Terry Company, 65 Spring Lane, Farmington, CT 06032, USA, http://www.fletcher-terry.com/.

8. Thermo Nicolet Corporation, 5225 Verona Road, Madison, WI 53711, USA, http://www.thermo.com/.

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